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MS-7817

ATX

Ver: 2.0

Intel -ShakeBay plamform

CPU:

INTEL-Haswell LGA1150

CPU DISPLAY

HDMI(portB) DVI (port C)

System Chipset:

INTEL-LYNX

OnBoard Chipset:

HD Audio Codec:ALC887 Co-lay 892

LAN-RTL8111G Co-lay 8106G

SIO:Nuvoton NCT6779

Main Memory:

DDRIII (1066/1333/1600MHz) \* 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1) Slot \* 2

PCI Slot \* 1

PWM:

VRD12 - ISL95812( 3 Phase 12MOS , Power pak)

Other:

SATA3 \*4

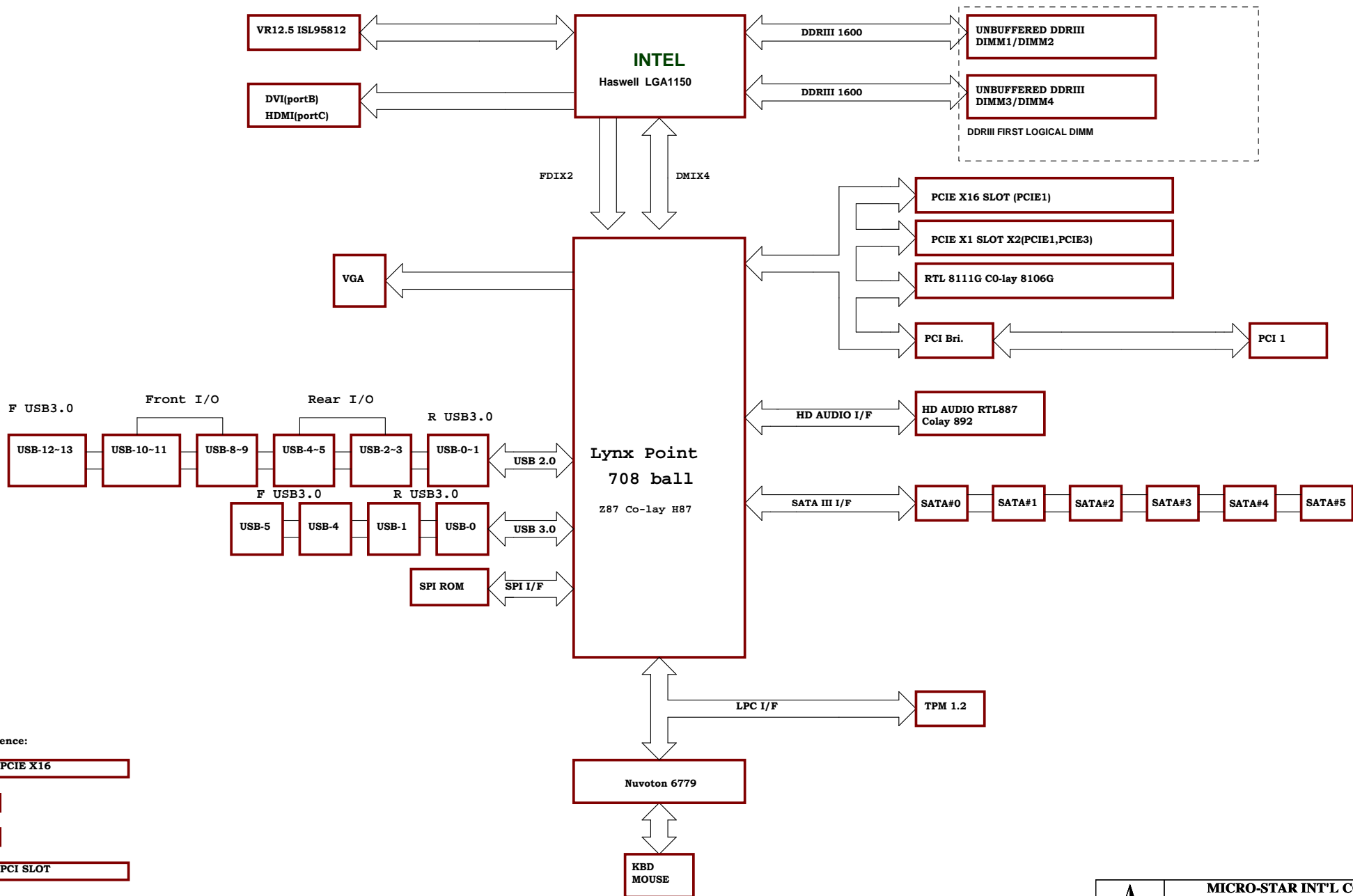
SATA2 \*2

REAL USB2.0 \*4

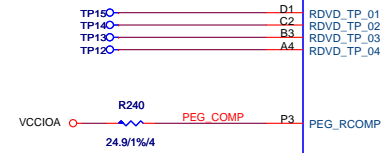
FRONT USB2.0 \*4

REAL USB3.0 \*2

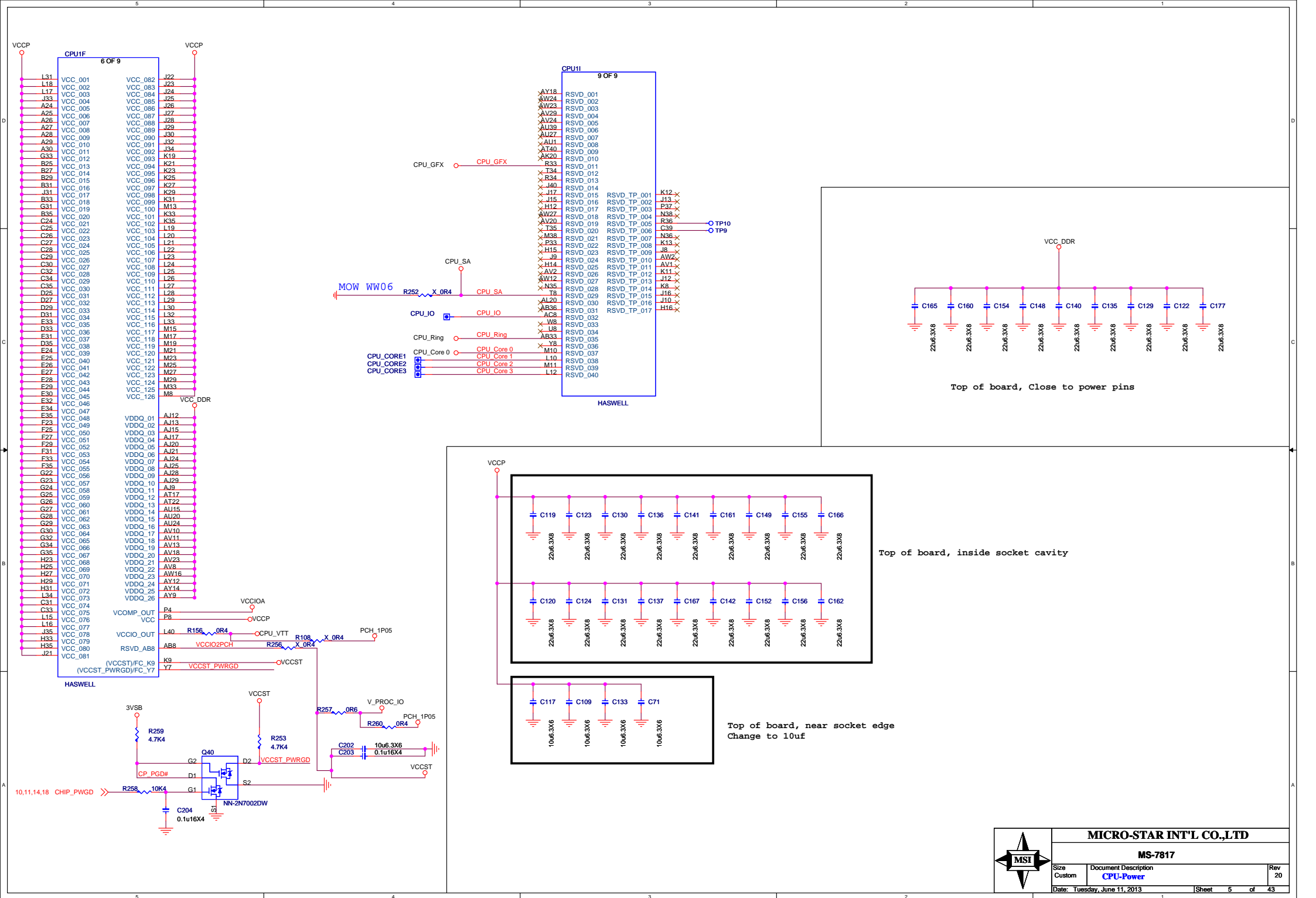
FRONT USB3.0 \*2



- Slot Sequence:
- PCIE X16
  - PCIE X1
  - PCIE X1
  - PCI SLOT

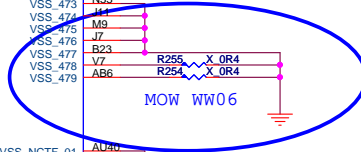






GND

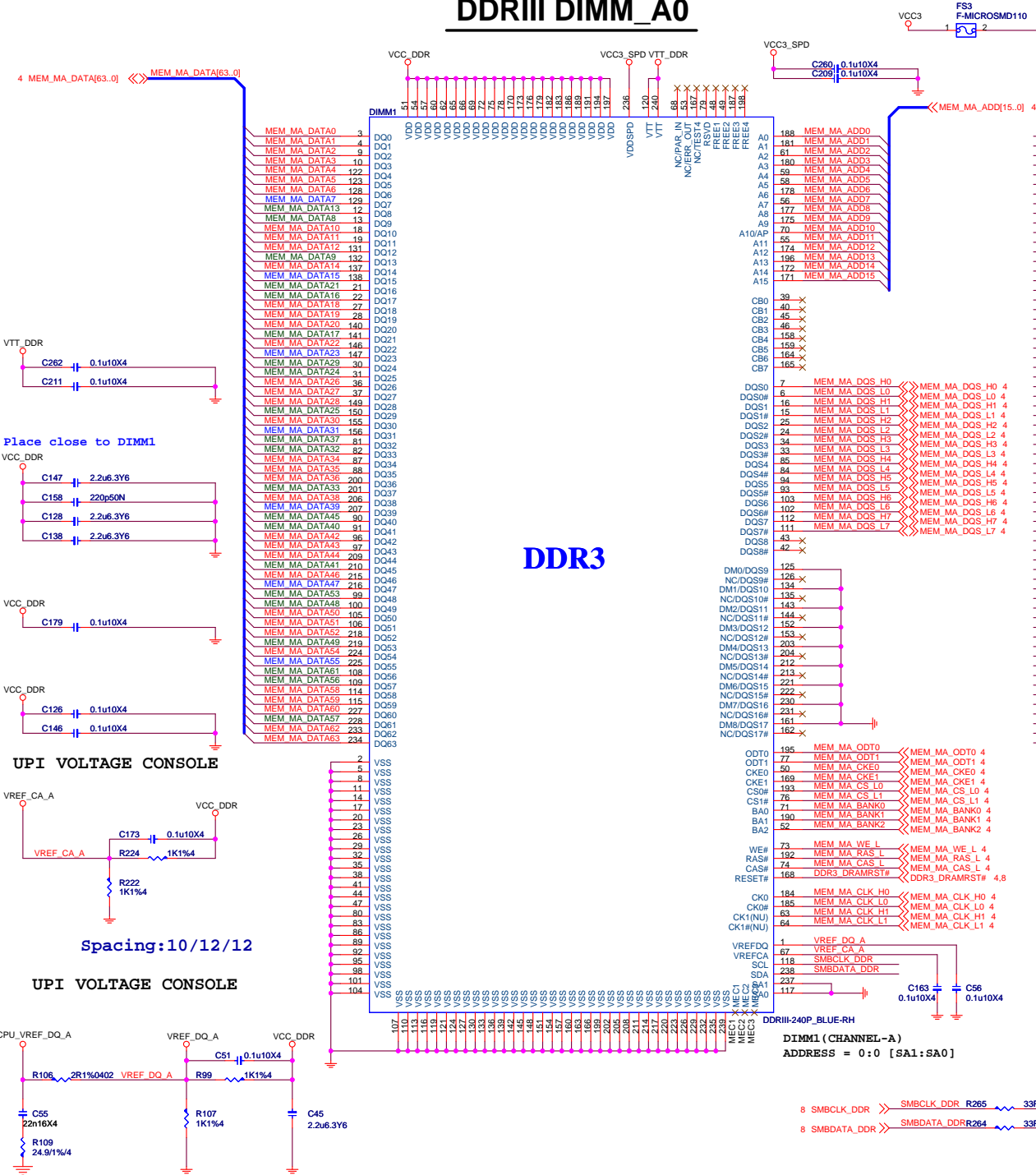
GND



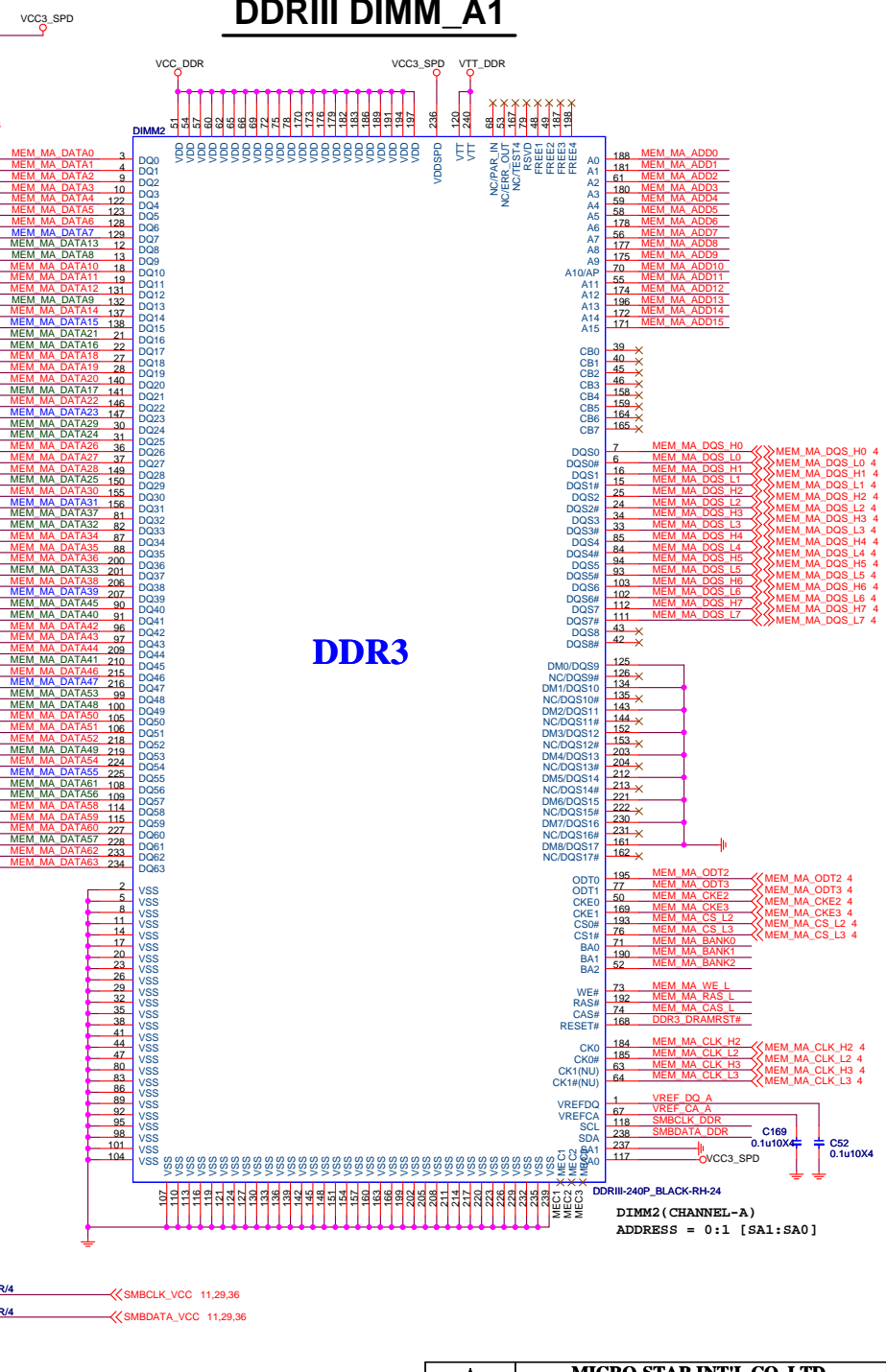
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## DDRIII DIMM A0



## DDRIII DIMM A1

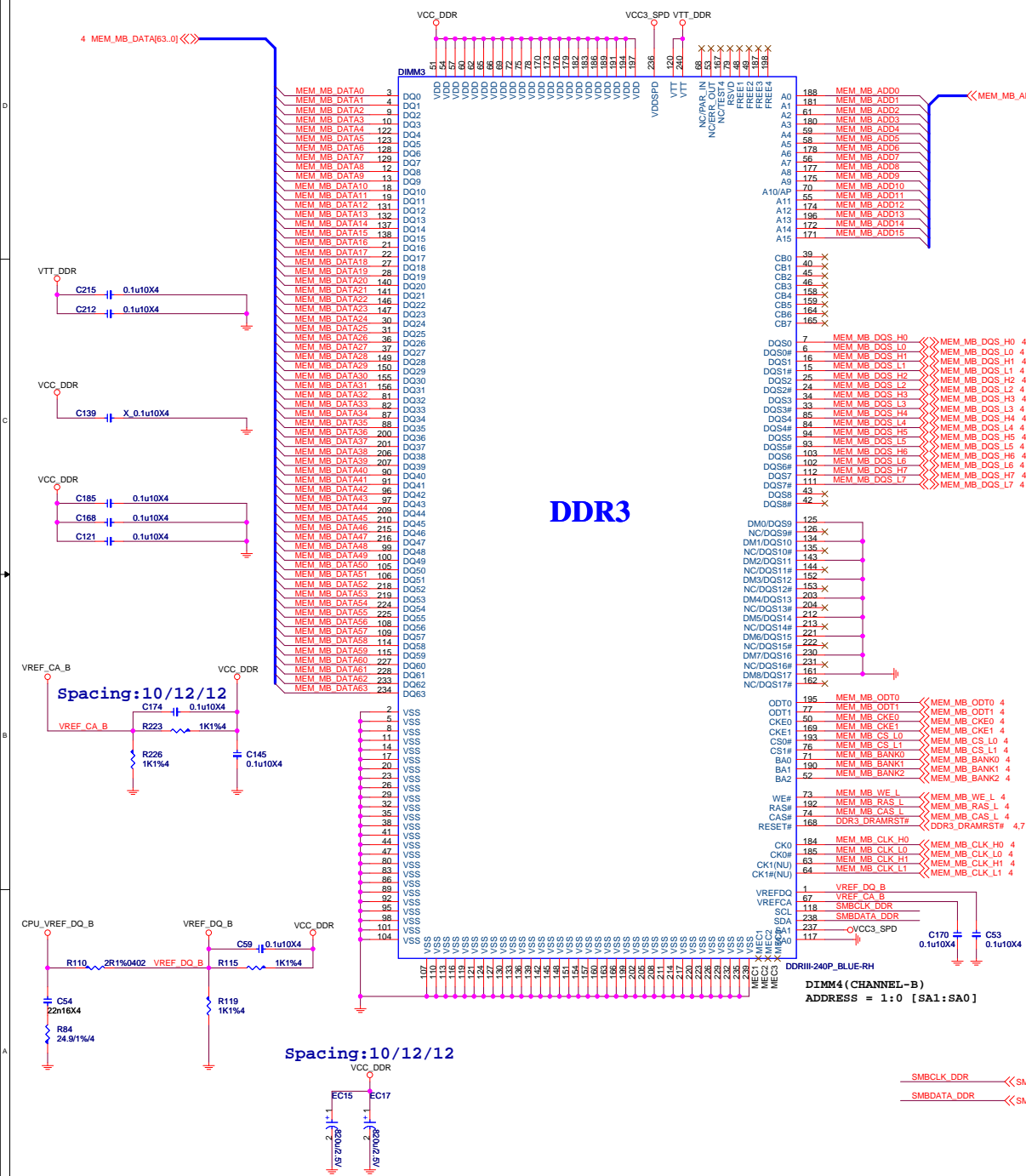


**MICRO-STAR INT'L CO.,LTD**

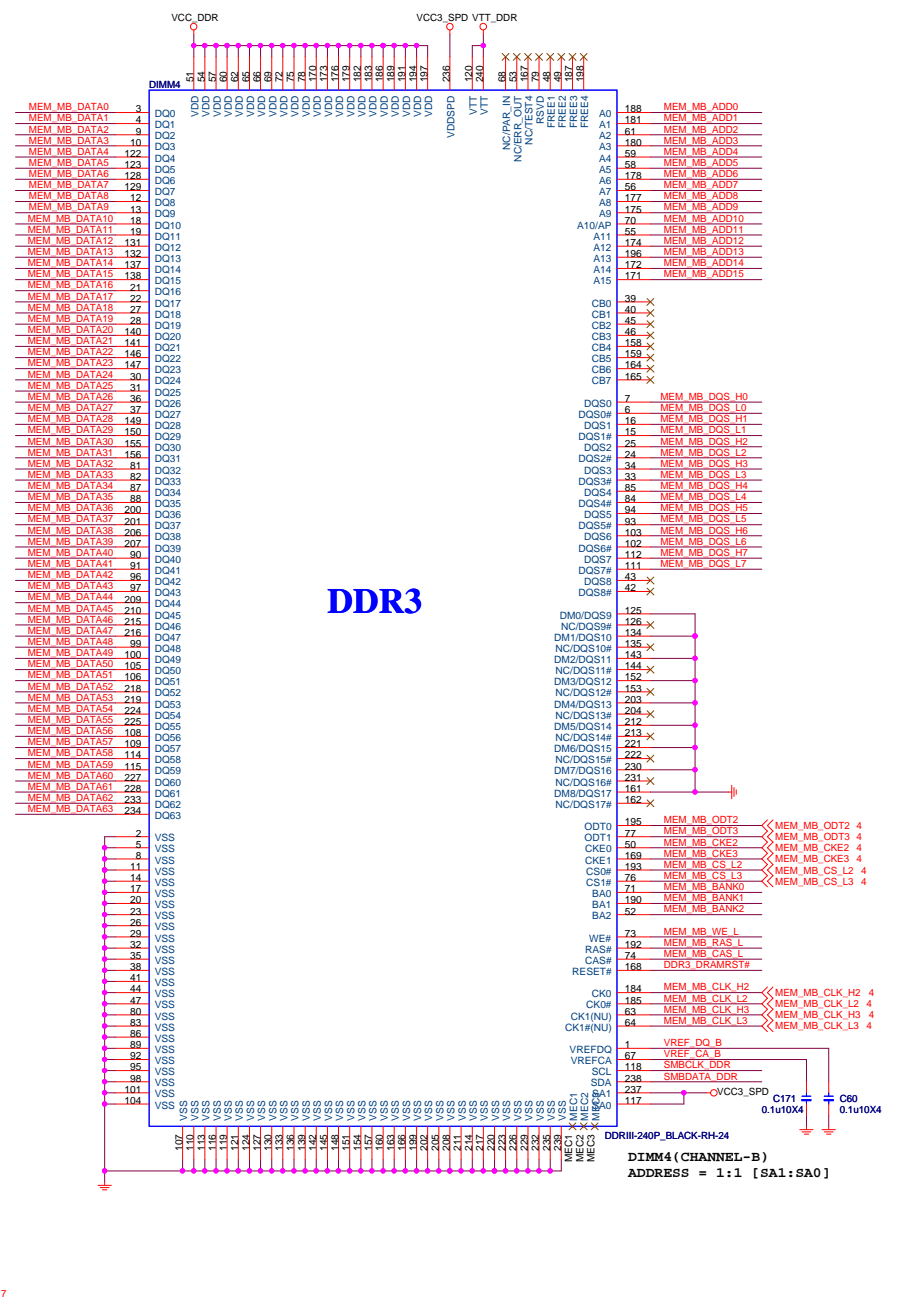
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## DDRIII DIMM\_B0



## DDRIII DIMM\_B1

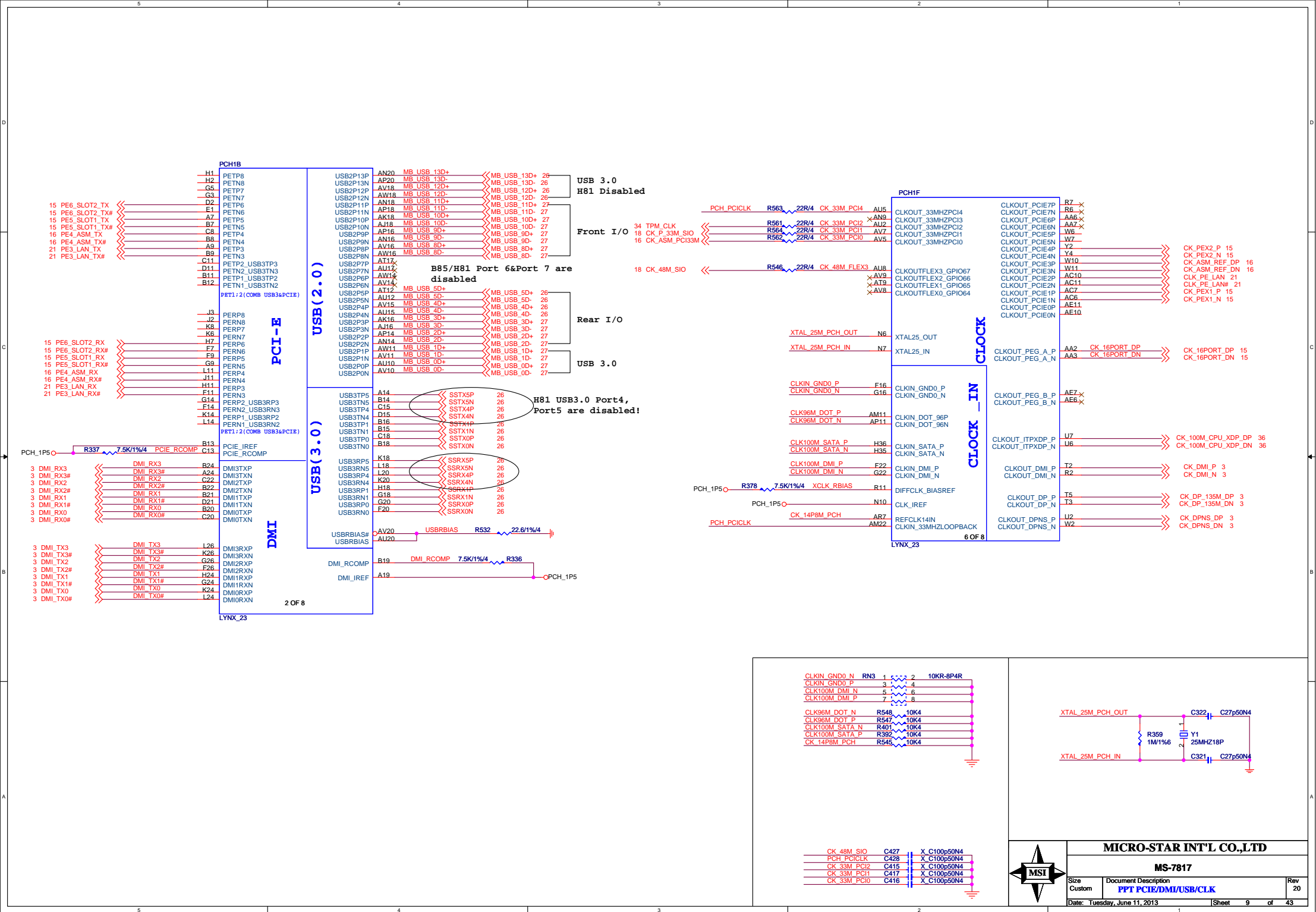


**MICRO-STAR INT'L CO.,LTD**

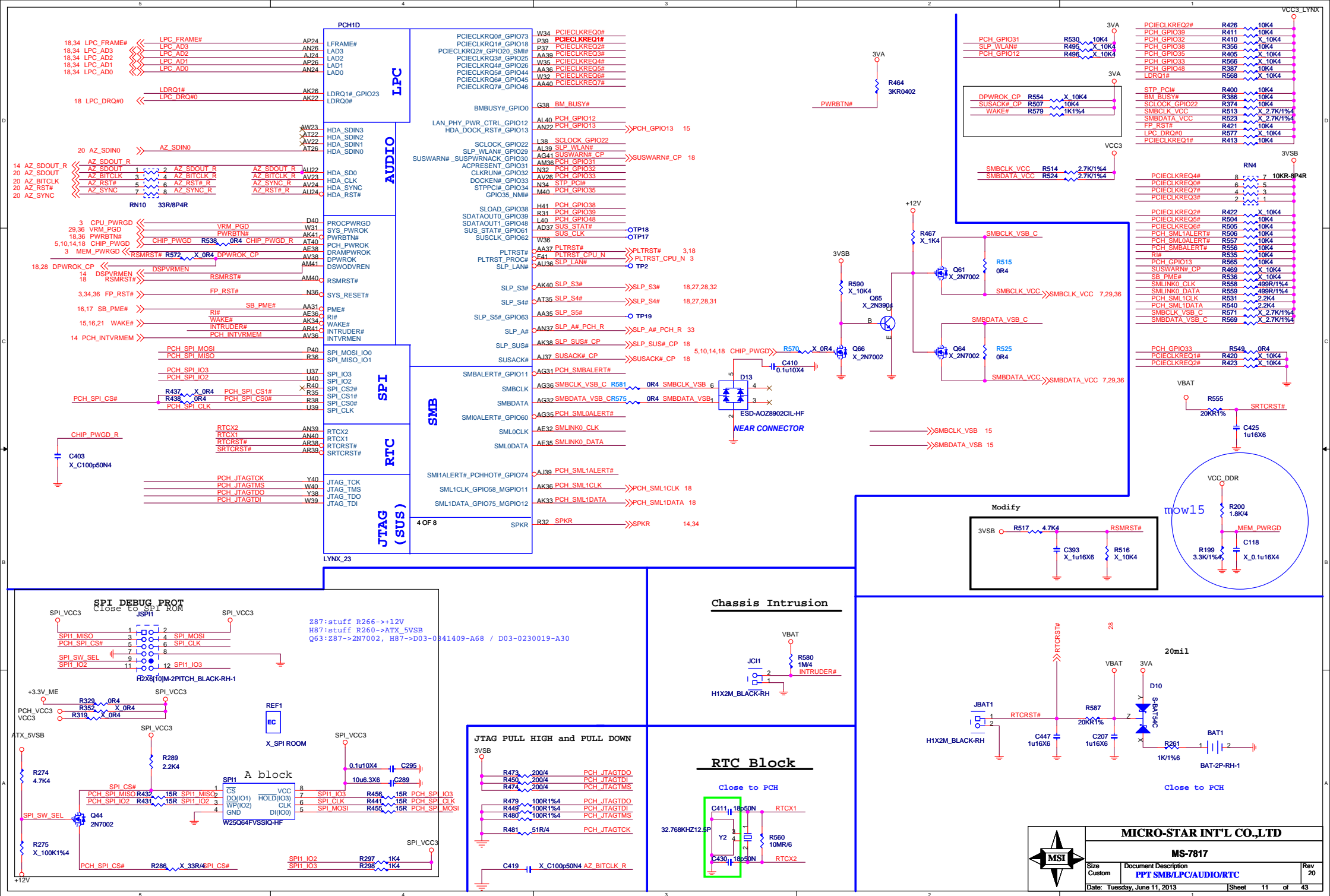
MS-7817

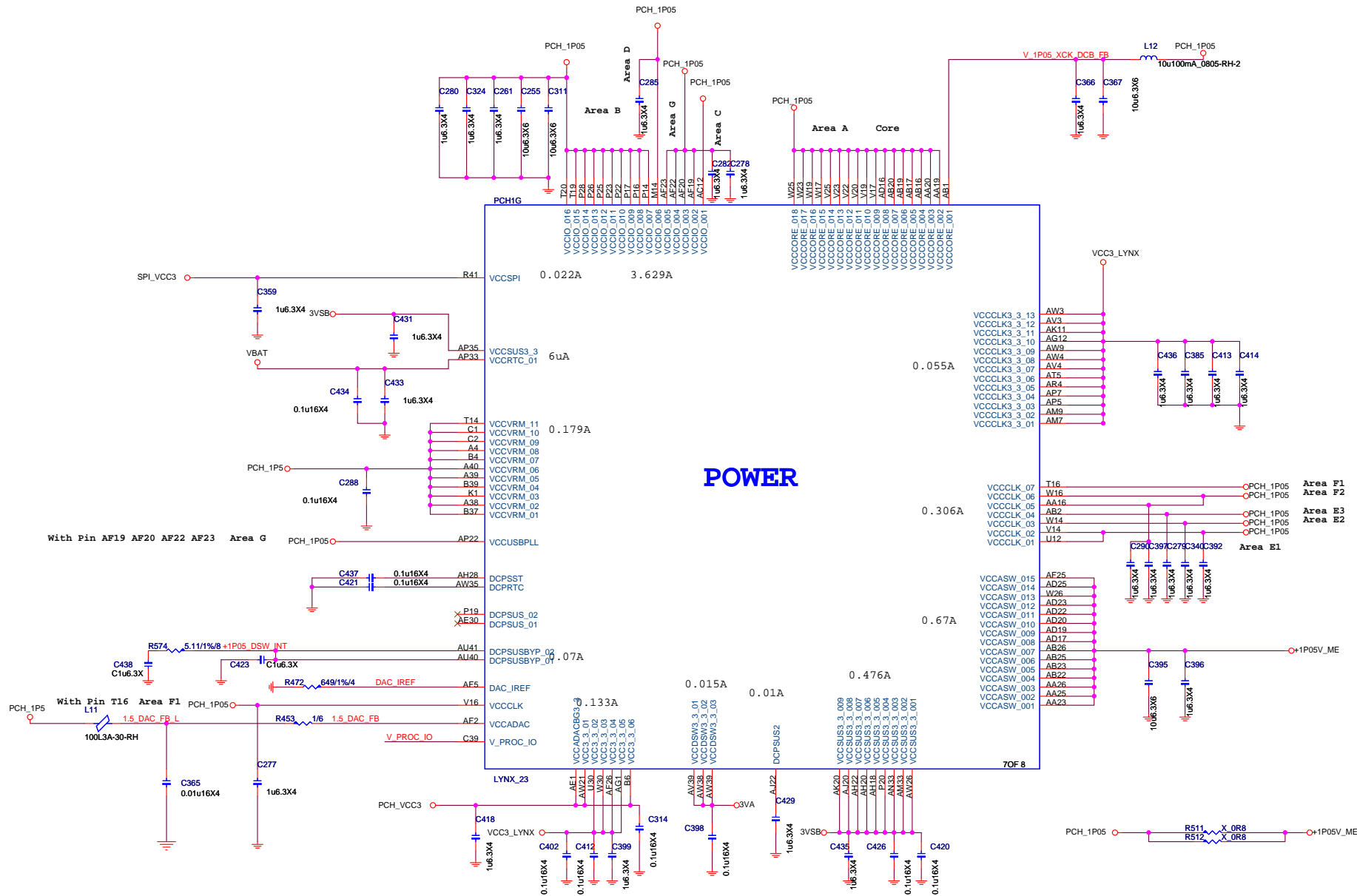
Size Custom	Document Description <b>DDR III B DIMM 1</b>	Rev 20
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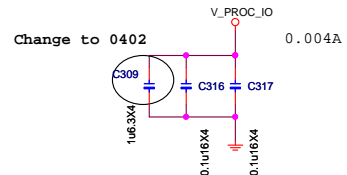
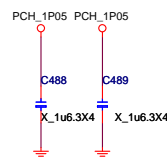


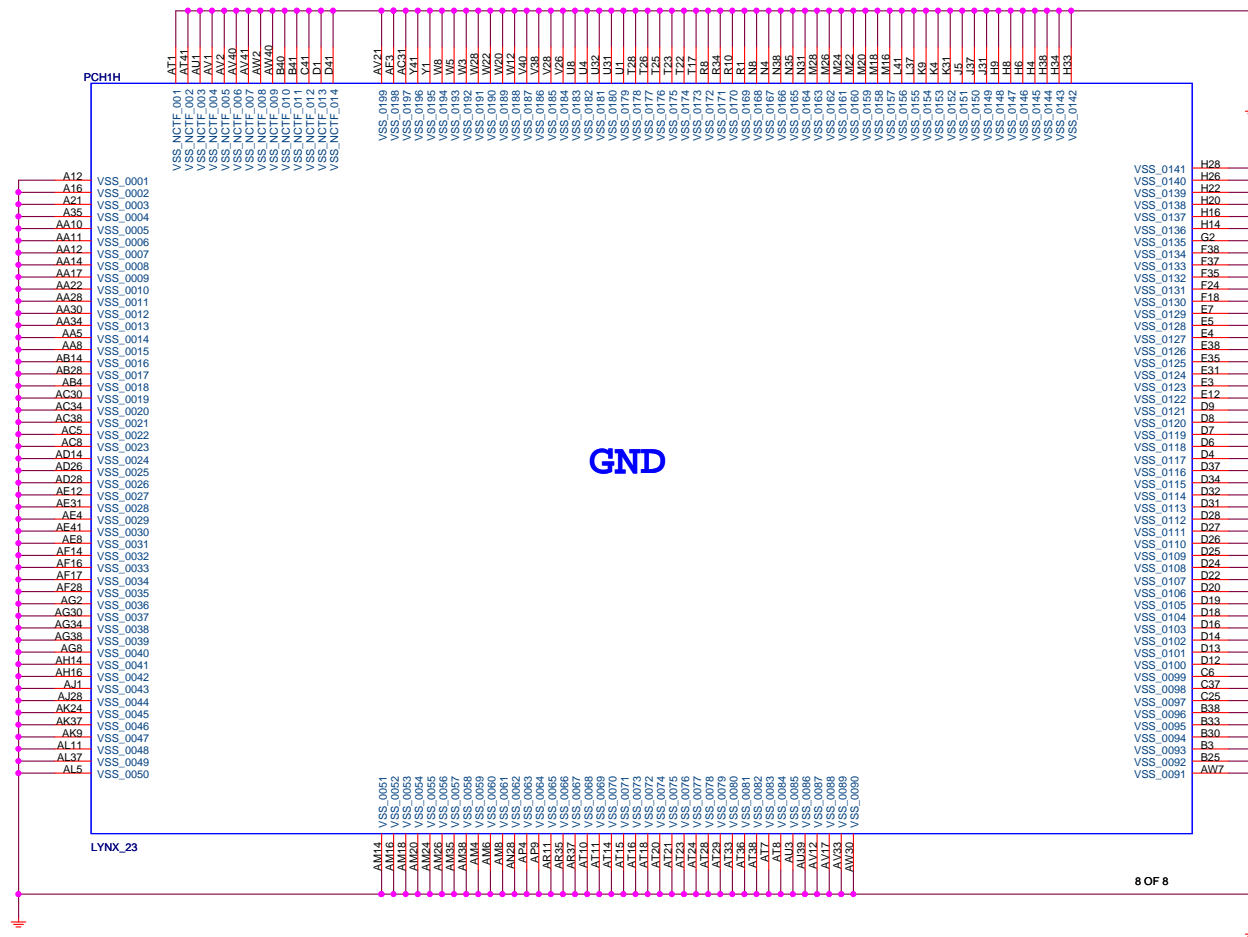






Backside for V14,U12,T16,V16  
unstuff





11 PCH INTVRMEM // PCH INTVRMEM R544 390K/4 VBAT

11 DSPVRMEN << DSPVRMEN R497 390K/4 VBAT

11,34 SPKR

SPKR R417 X 8.2K/4

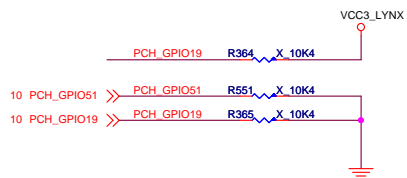
Internal pull-DOWN

VCC3\_LYNX

10 PCH\_GPIO55 >> PCH\_GPIO55 R537 X 4.7K4

Internal pull-up

Default



10 PCH\_GPIO53 >> PCH\_GPIO53 R552 X 1K4

Leave NC. internal pull down.

3VSB

R454 X 1K1%

C393 X 1K1%

VCC3\_LYNX

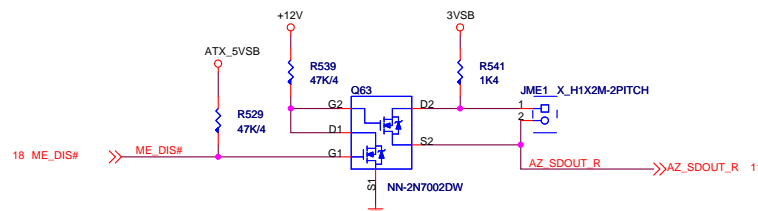
10 PCH\_GPIO37 >> PCH\_GPIO37

PCH\_GPIO37

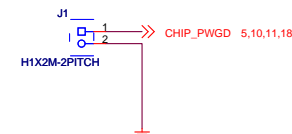
R397 X 10K4

VCC3 Follow VCC3

Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.



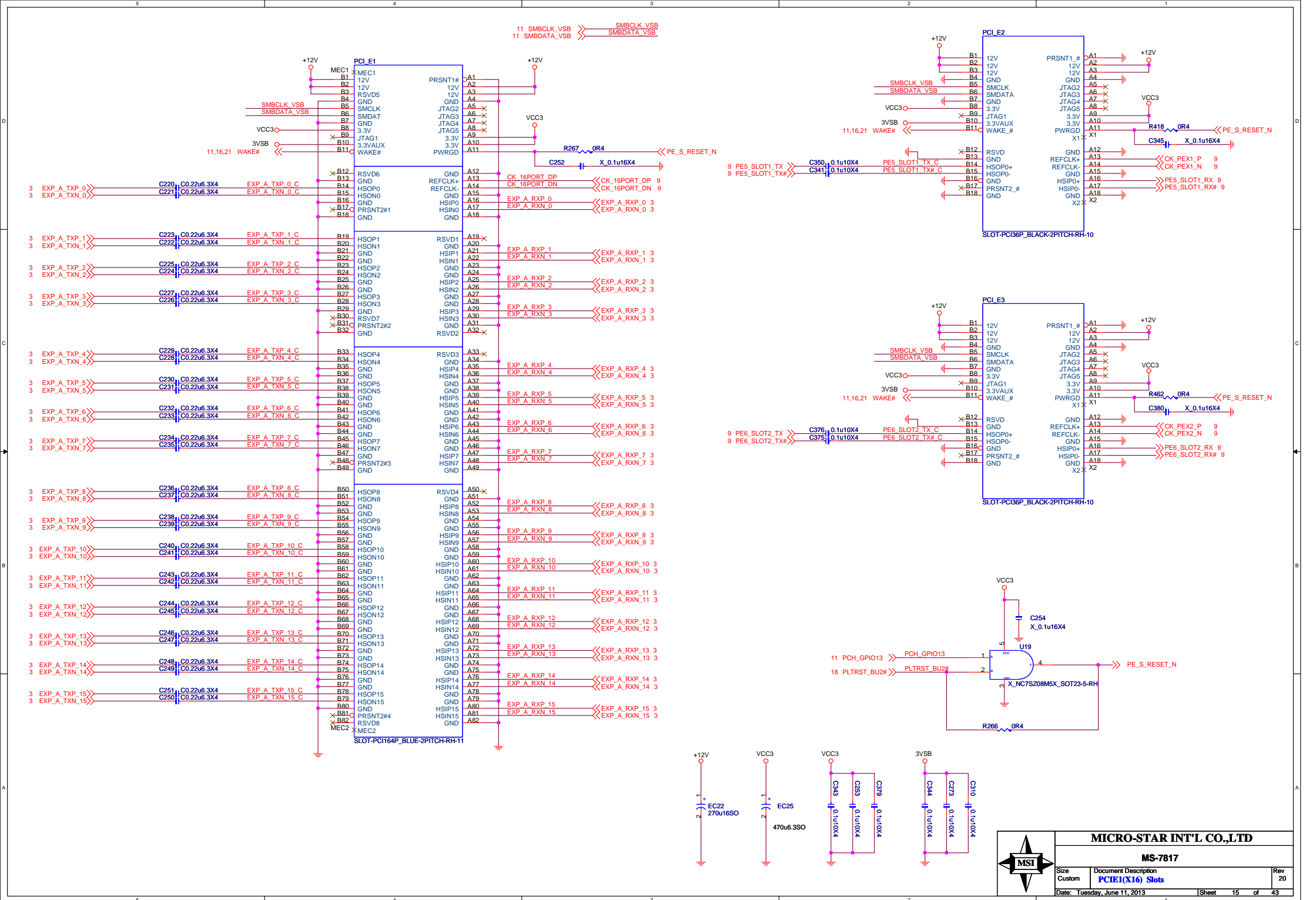
For test cpu voltage

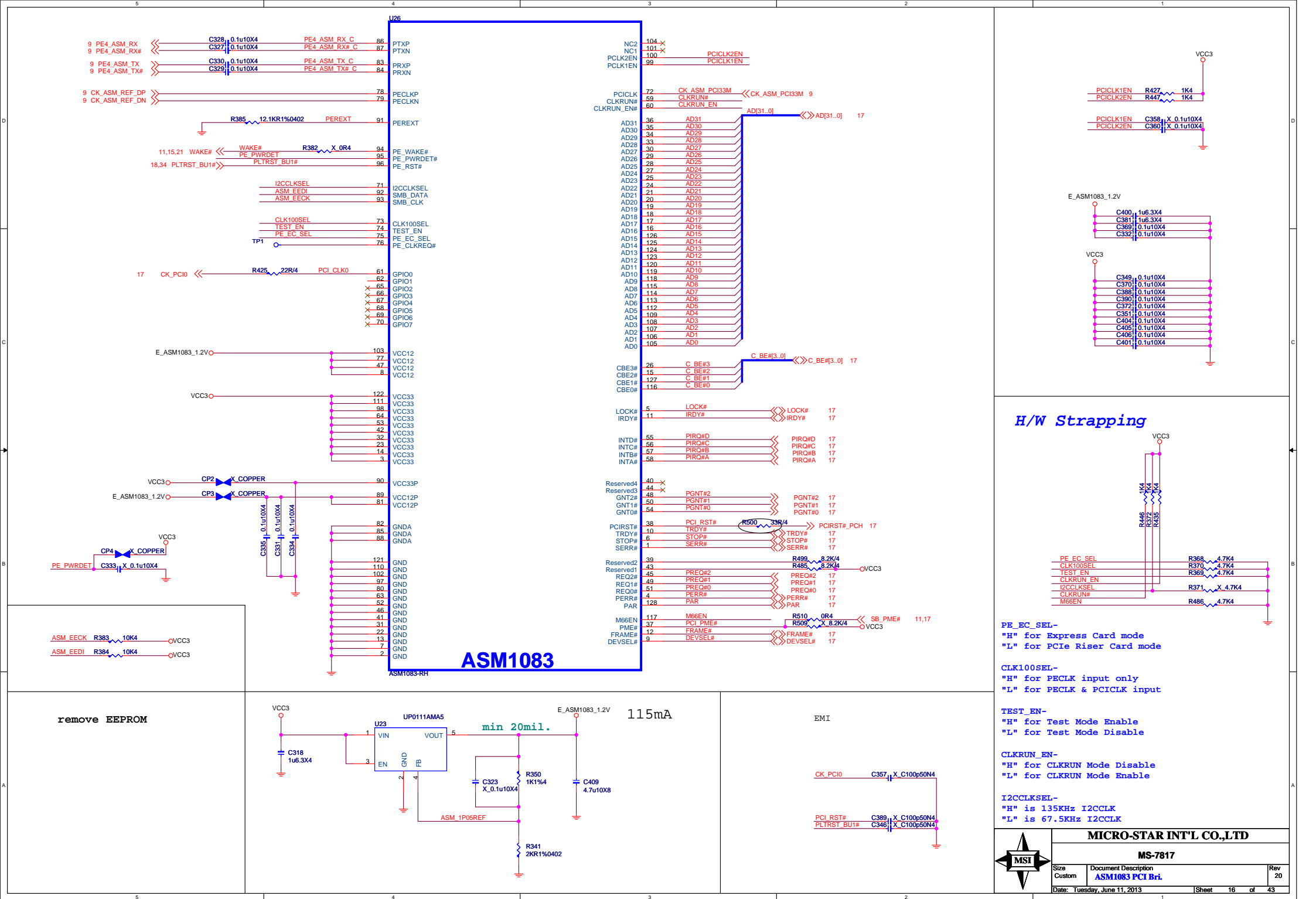
[illegible]

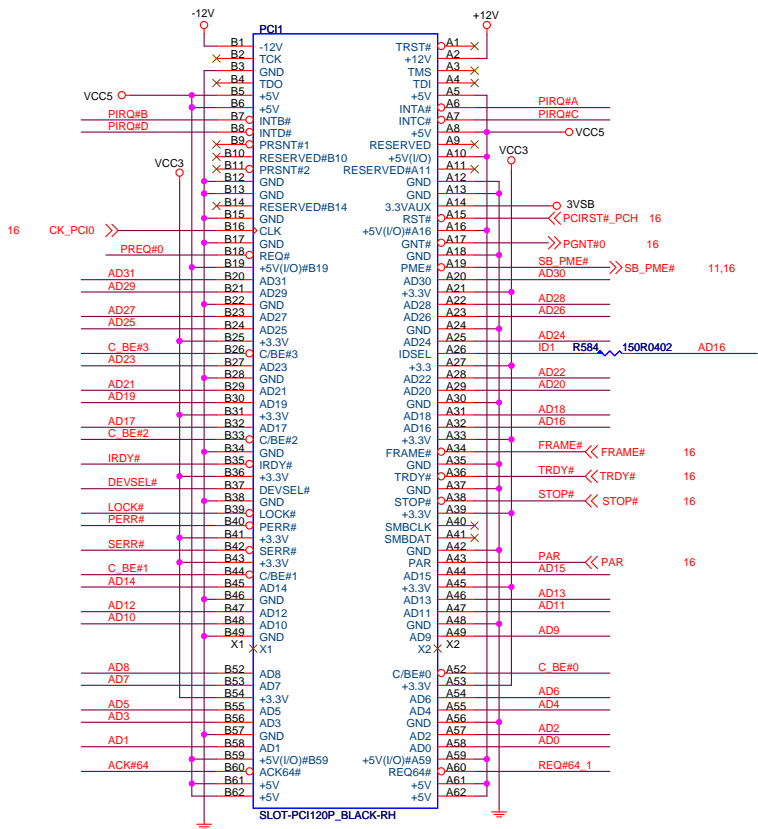
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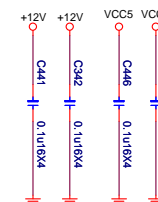
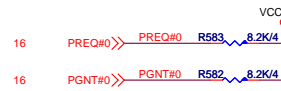
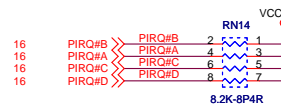
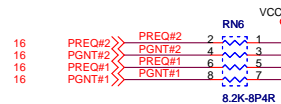
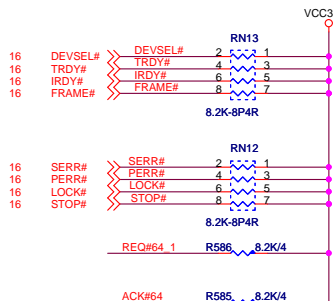
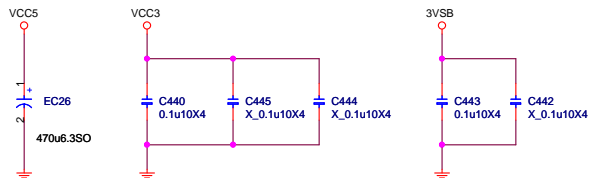


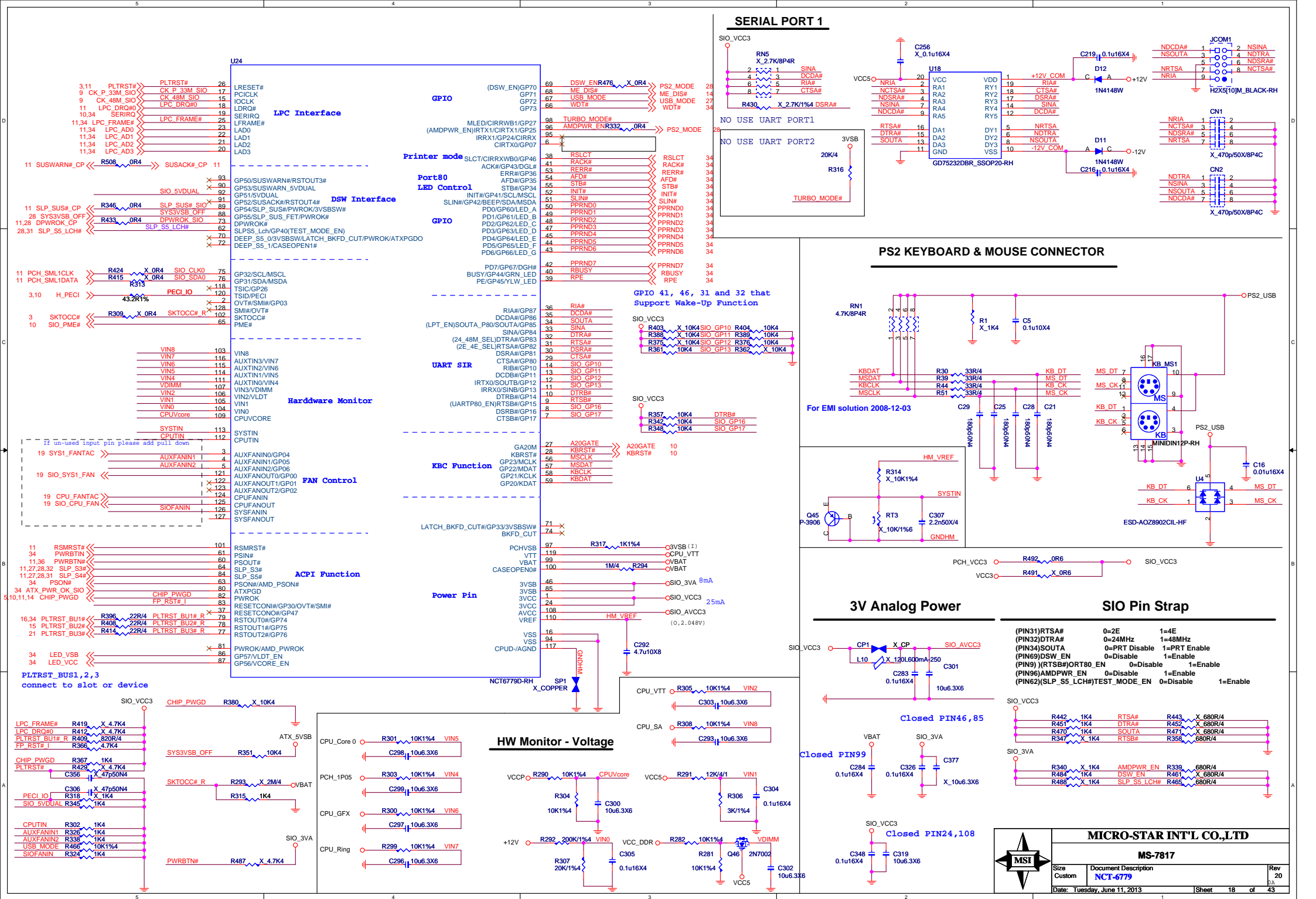


**IDSEL = AD16**  
**MASTER = PREQ#0**  
**PIRQ#A**

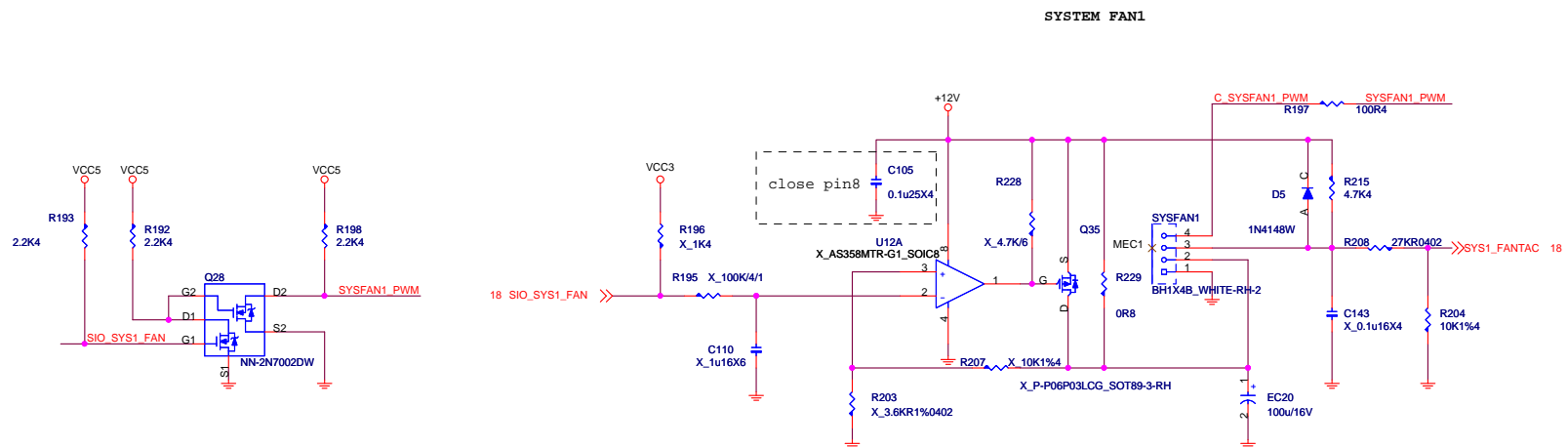
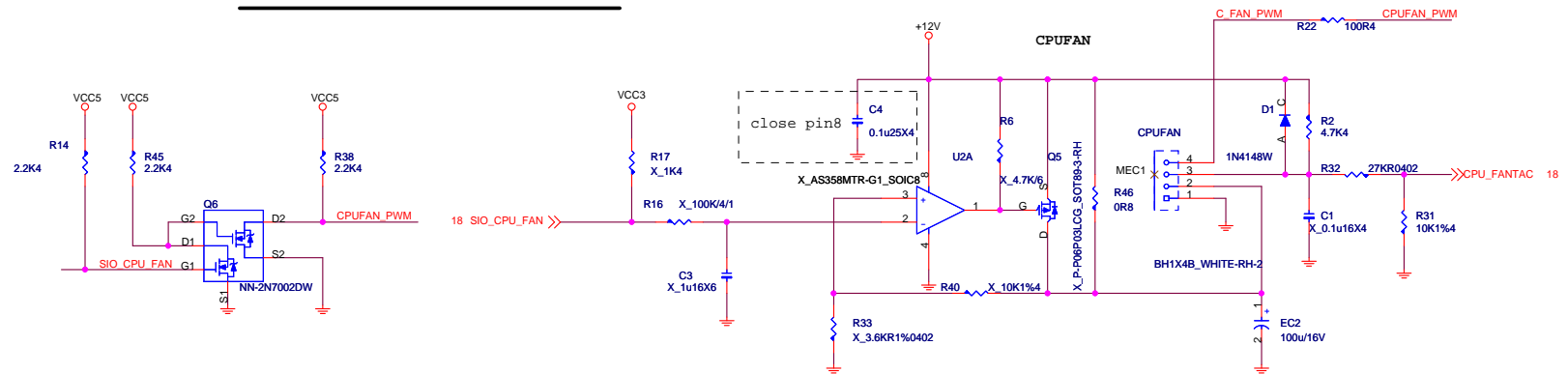
AD[31..0] <<> AD[31..0] 16  
 C\_BE#[3..0] <<> C\_BE#[3..0] 16

### PCI PULL-UP / DOWN RESISTORS

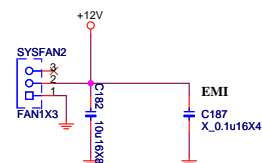




# FAN-COUNTROL CIRCUIT



SYSTEM FAN1

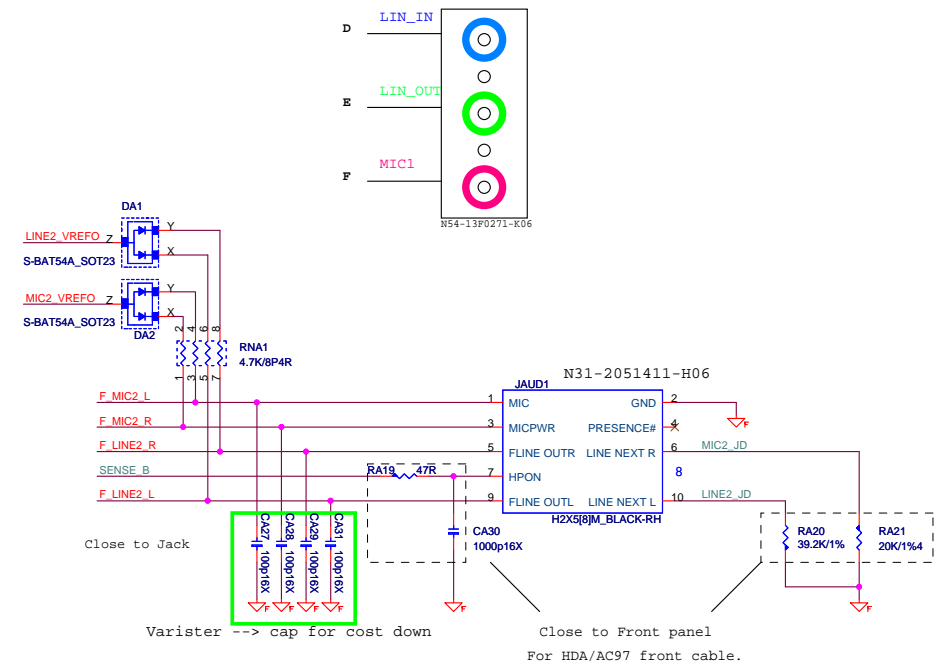
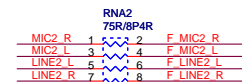
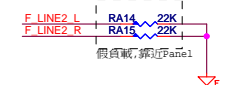
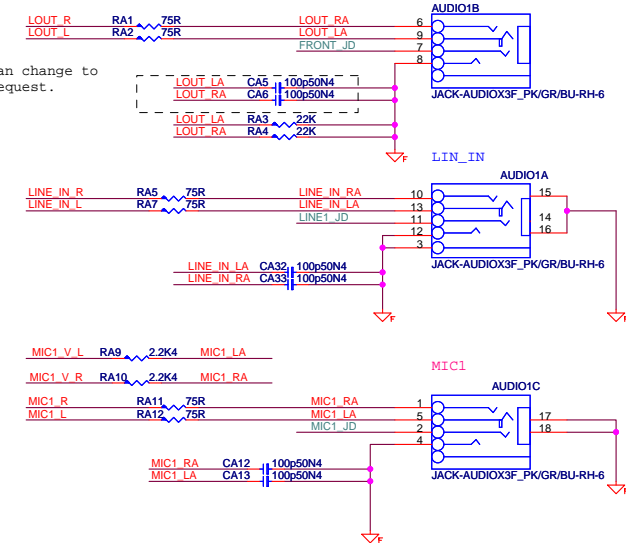
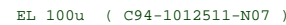


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## VT1708S CE



**MICRO-STAR INT'L CO.,LTD**

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Size Custom	Document Description <b>Audio Codec ALC887</b>
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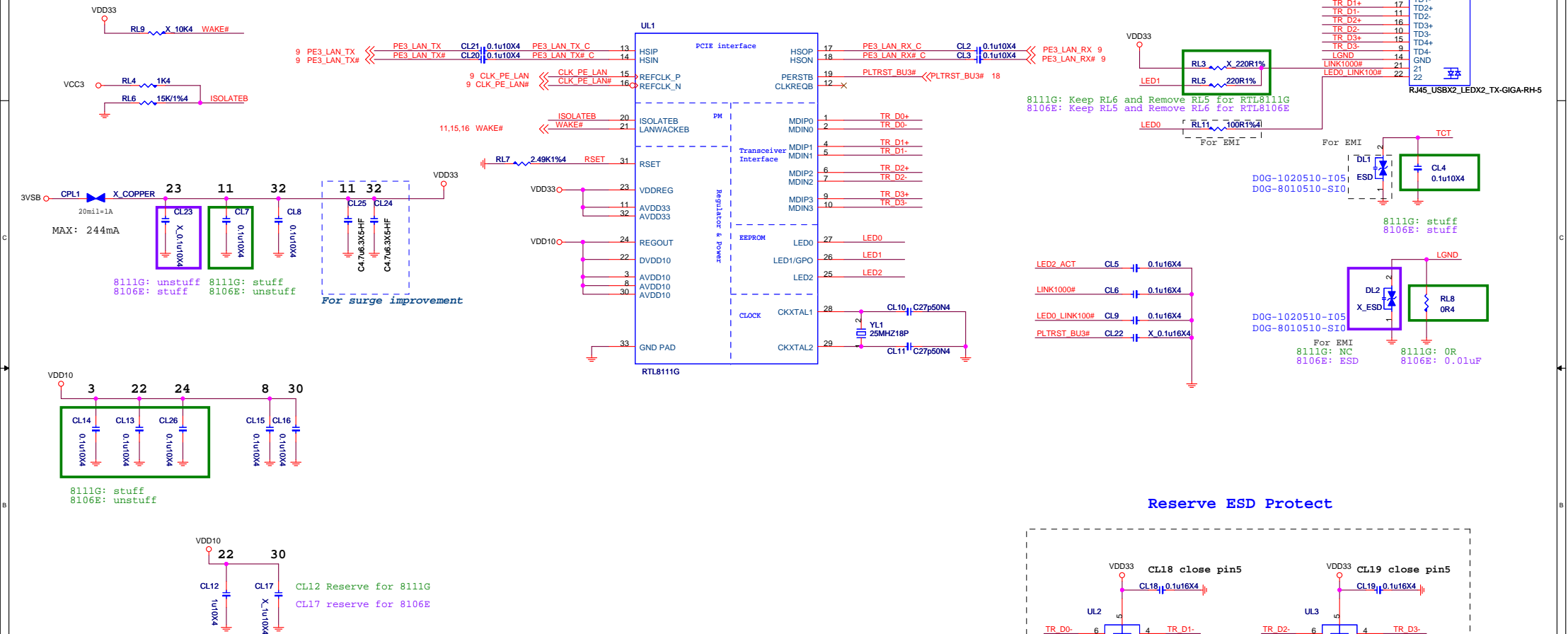
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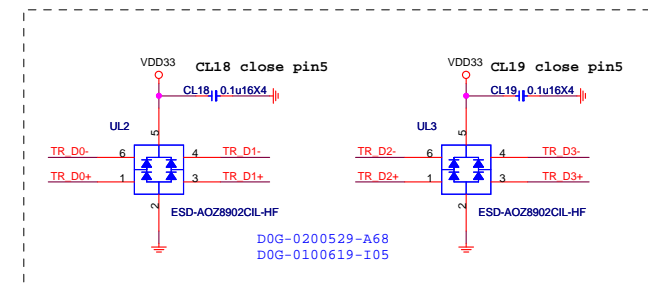
# RTL8111G Giga LAN

## RTL8106E 10/100M LAN

### LAN Connector



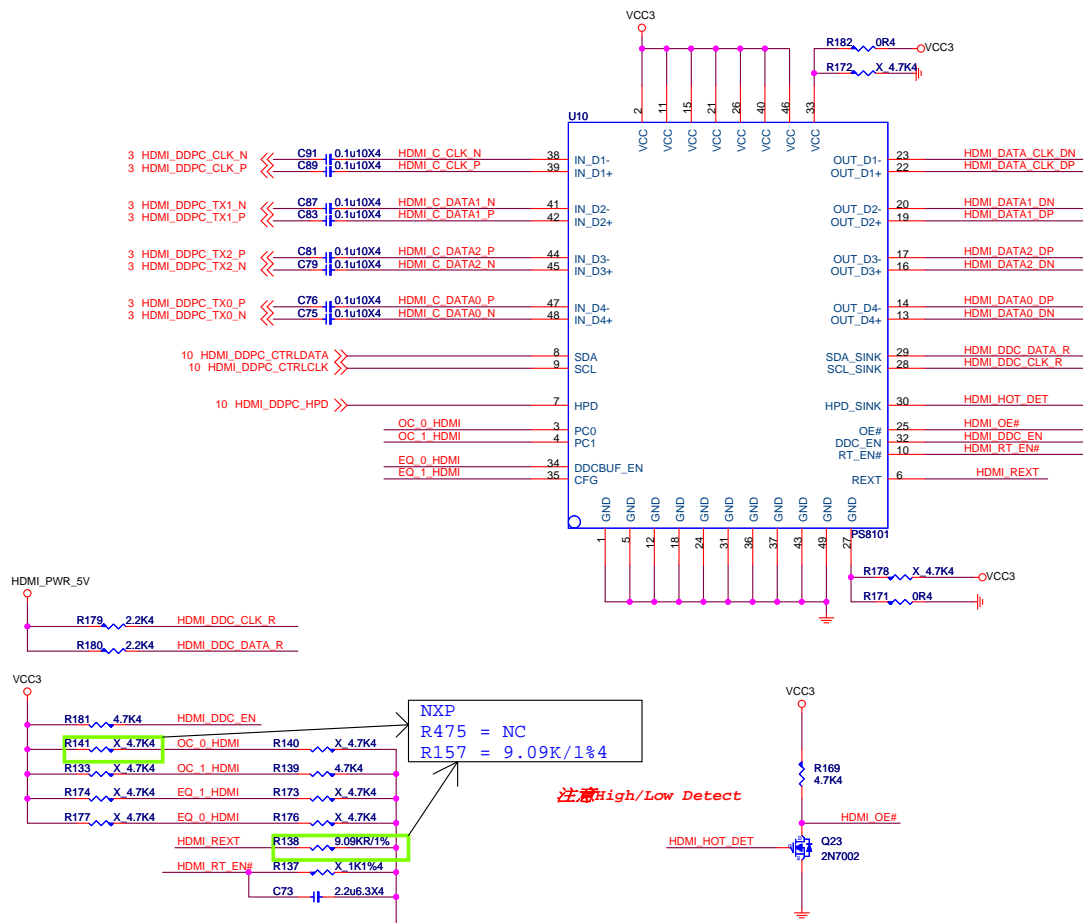
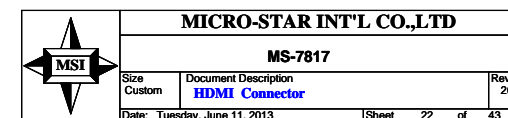
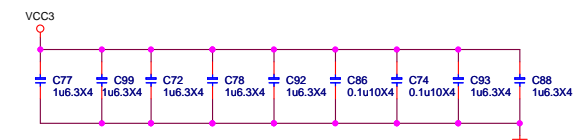
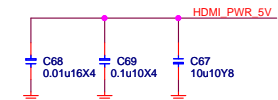
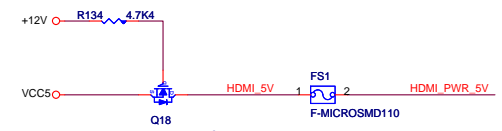
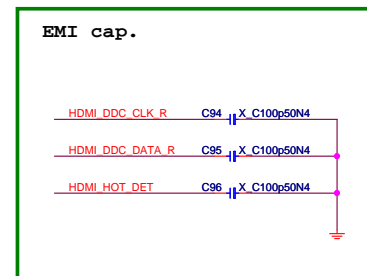
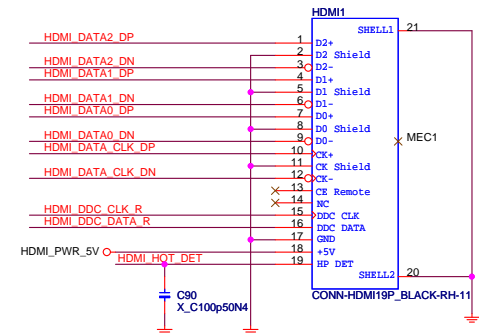
### Reserve ESD Protect



## HDMI level shifter

**Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings**

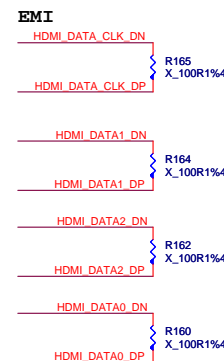
Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMD5B_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMD5B_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMD5B_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMD5B_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMD5B_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMD5B_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMD5B_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMD5B_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
SDVO_CTRLCLK	HDMI5_CTRL_CLK	HDMI DDC lines for Port B	
SDVO_CTRLDATA	HDMI5_CTRL_DATA		



	"0"	"1"
DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

{DDC_EN, DDCBUF_EN, OE#}	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PCI, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

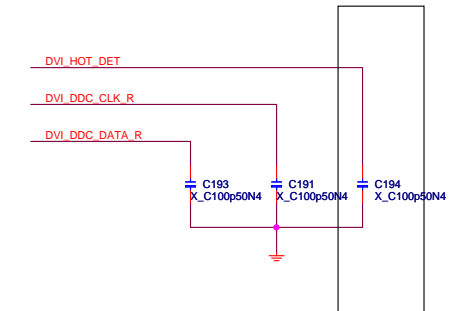
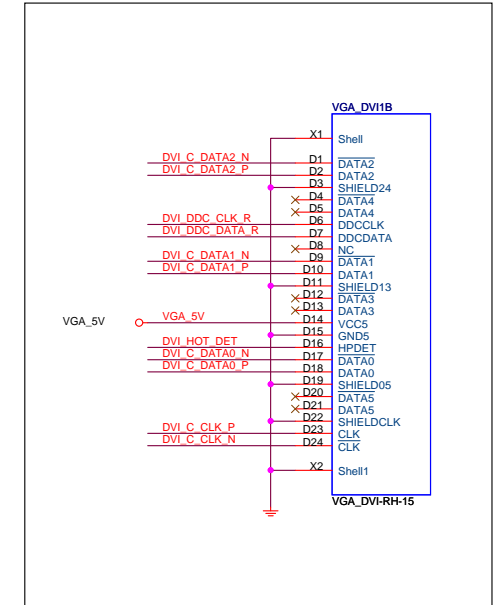
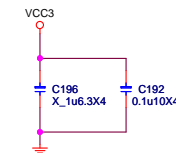
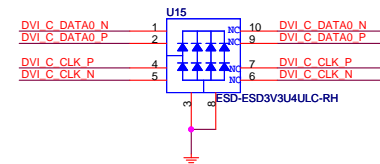
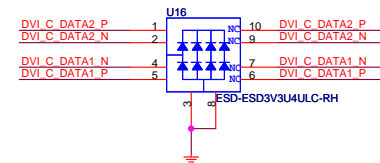
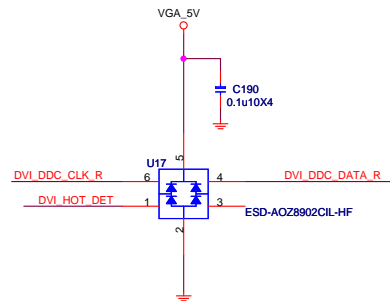
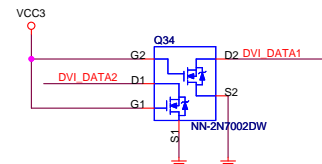
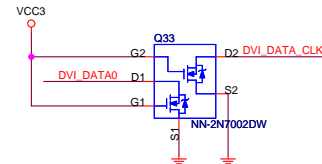
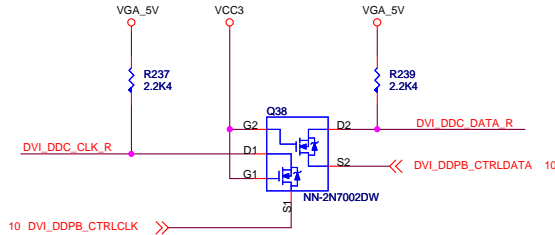


VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

3 DVI\_DDPB\_CLK\_N C132 0.1u10X4 DVI\_C\_CLK\_N R205 470R0402  
 3 DVI\_DDPB\_CLK\_P C134 0.1u10X4 DVI\_C\_CLK\_P R209 470R0402  
 3 DVI\_DDPB\_TXN0 C150 0.1u10X4 DVI\_C\_DATA0\_N R214 470R0402  
 3 DVI\_DDPB\_TXN0 C144 0.1u10X4 DVI\_C\_DATA0\_P R211 470R0402  
 3 DVI\_DDPB\_TXN1 C157 0.1u10X4 DVI\_C\_DATA1\_N R218 470R0402  
 3 DVI\_DDPB\_TXN1 C153 0.1u10X4 DVI\_C\_DATA1\_P R213 470R0402  
 3 DVI\_DDPB\_TXN2 C159 0.1u10X4 DVI\_C\_DATA2\_N R219 470R0402  
 3 DVI\_DDPB\_TXN2 C164 0.1u10X4 DVI\_C\_DATA2\_P R221 470R0402

For EMI

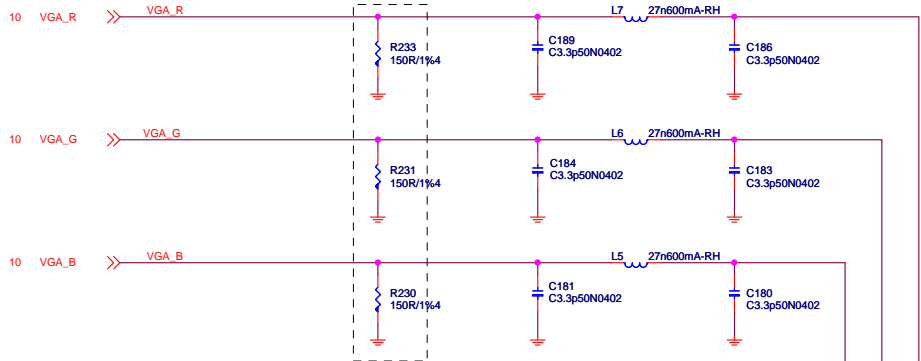
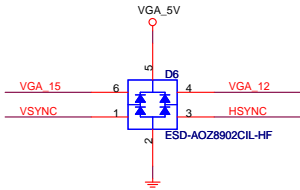
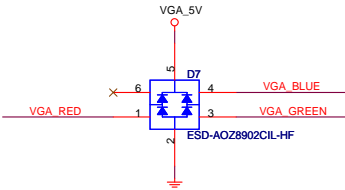
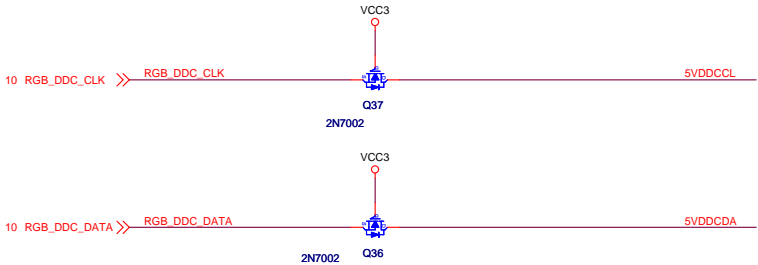
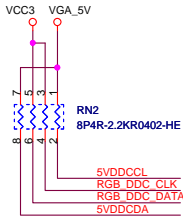
DVI\_C\_DATA0\_N R212 470R0402  
 DVI\_C\_DATA0\_P X\_243R1%0402  
 DVI\_C\_DATA1\_N R216 470R0402  
 DVI\_C\_DATA1\_P X\_243R1%0402  
 DVI\_C\_CLK\_N R206 470R0402  
 DVI\_C\_CLK\_P X\_243R1%0402  
 DVI\_C\_DATA2\_N R220 470R0402  
 DVI\_C\_DATA2\_P X\_243R1%0402



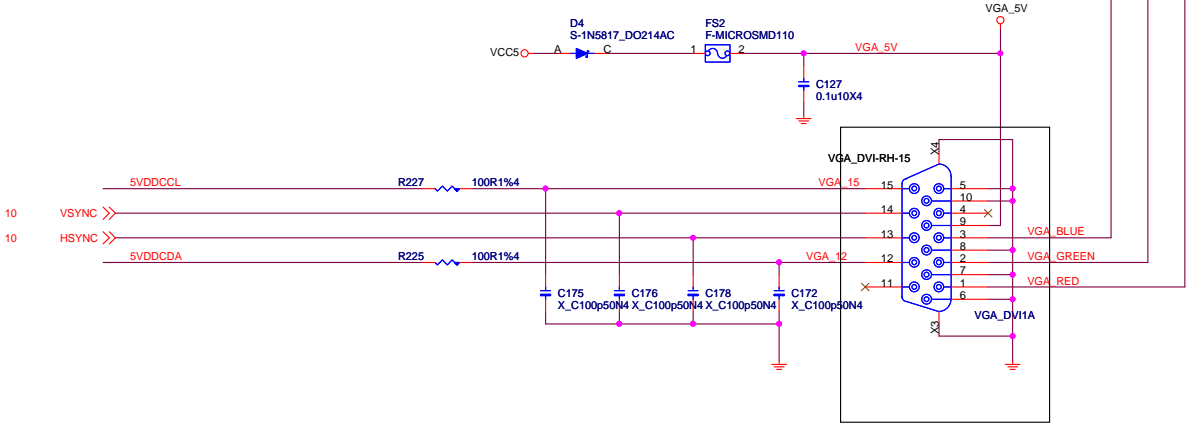
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift

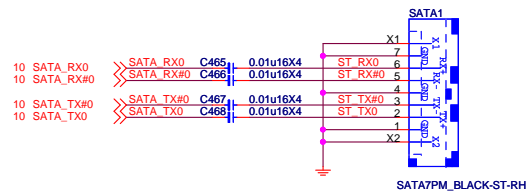


PLACE CLOSE TO VGA CONNECTOR,  
WITHIN 750 MIL OF PIN



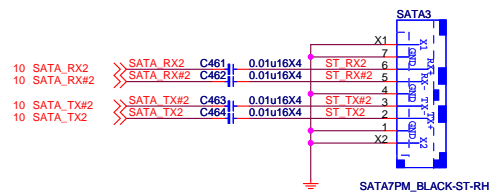
### SATA 6G PORT 0,1

3.0



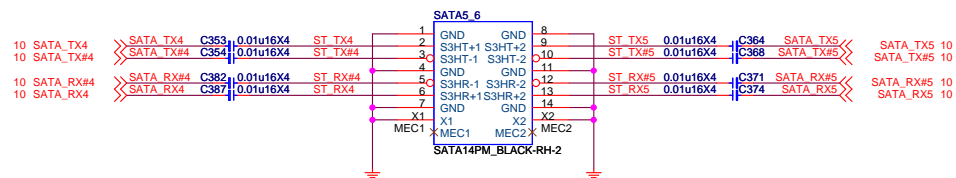
### SATA 6G PORT 2,3

3.0



### SATA 3G PORT 4,5

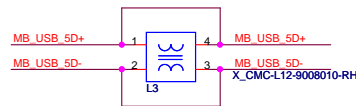
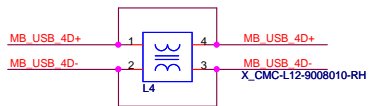
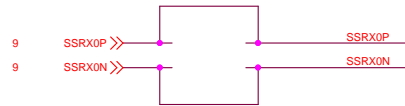
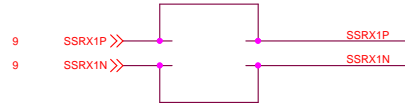
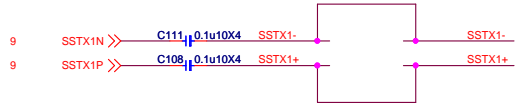
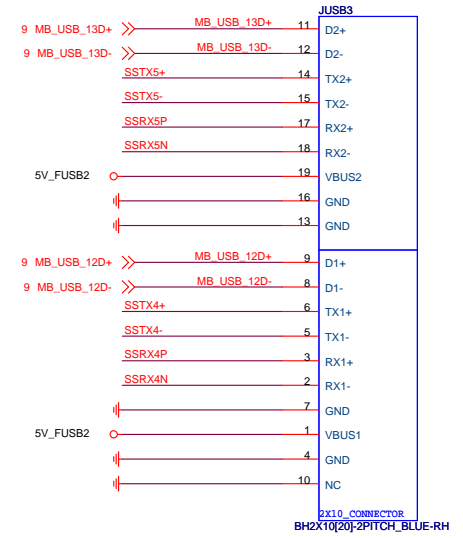
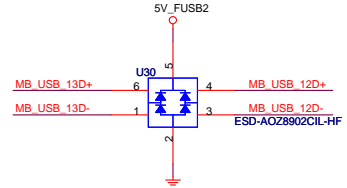
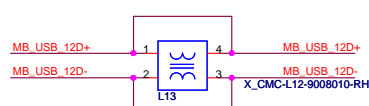
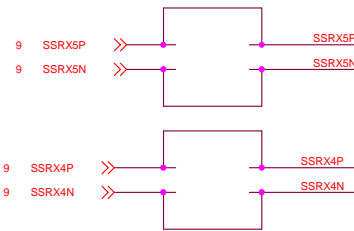
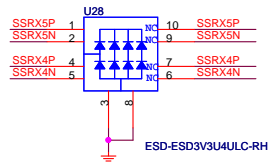
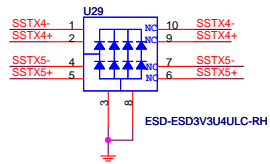
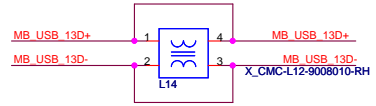
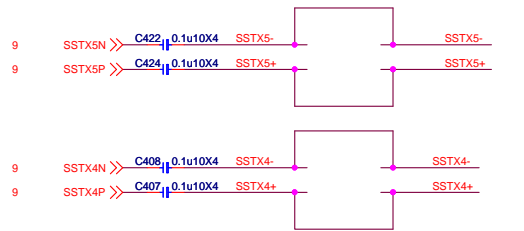
2.0



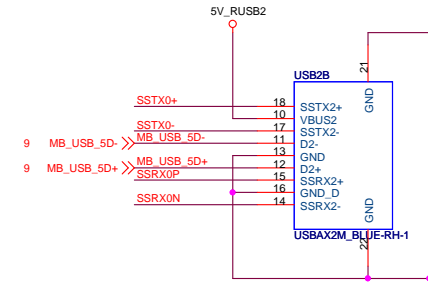
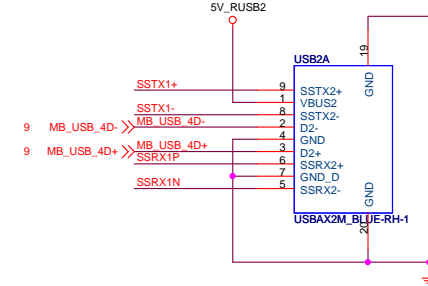
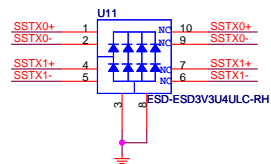
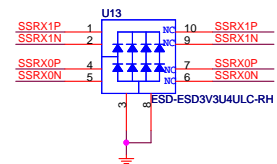
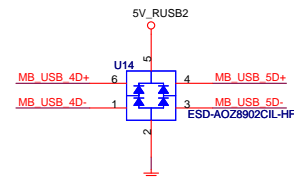
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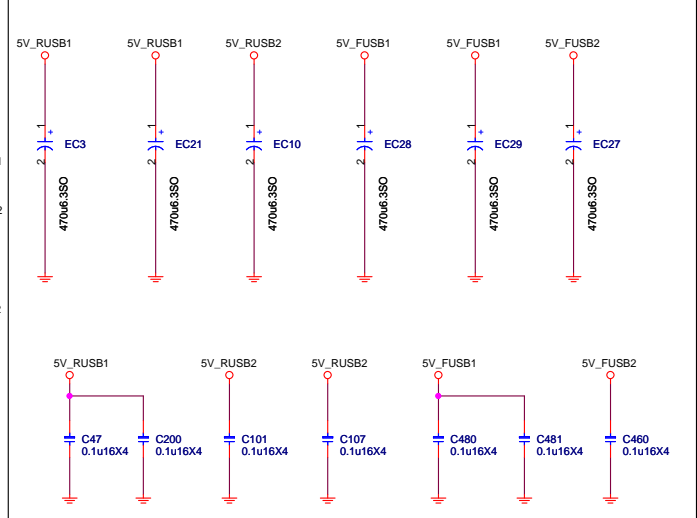
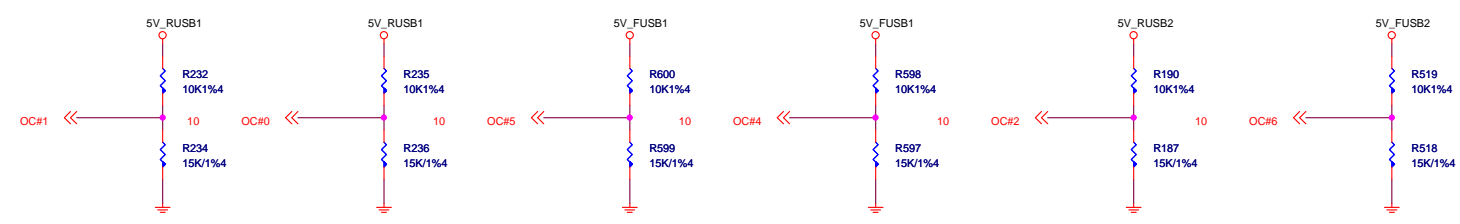
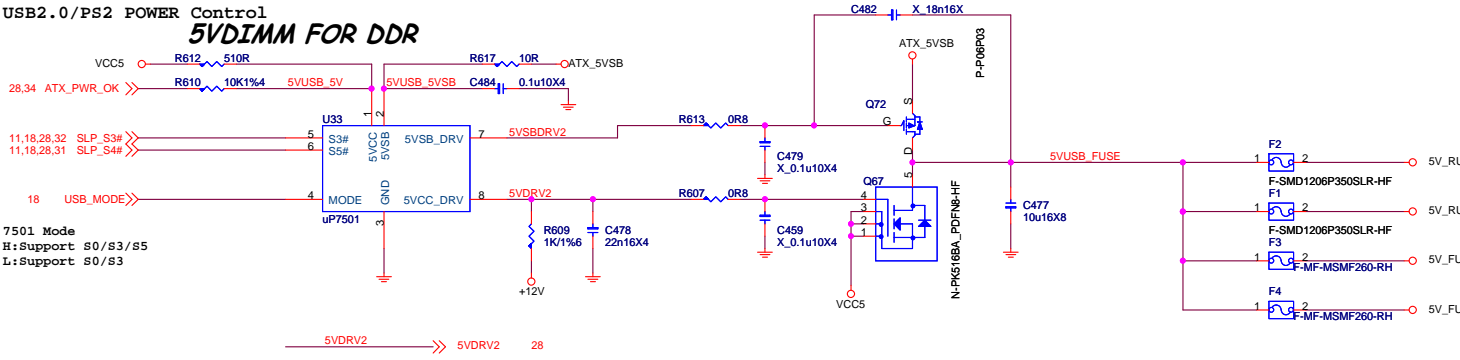
EMI



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USB2.0/PS2 POWER Control  
**SVDIMM FOR DDR**

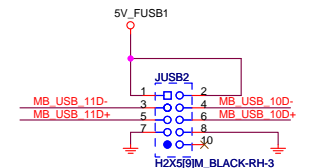
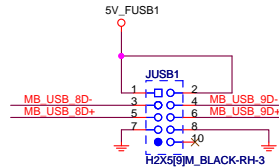
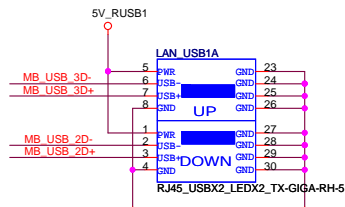
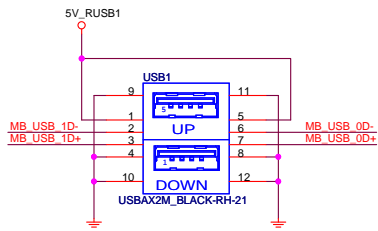
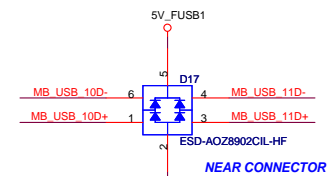
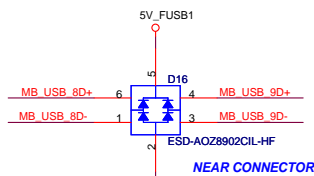
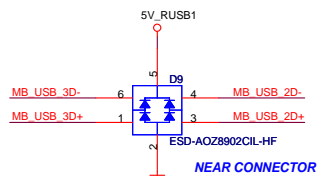
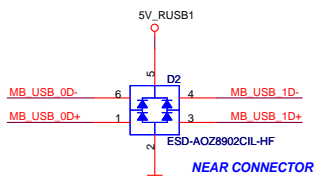
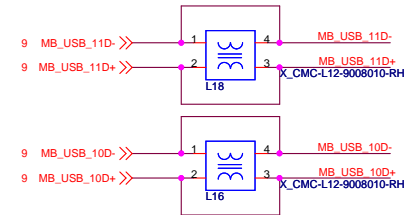
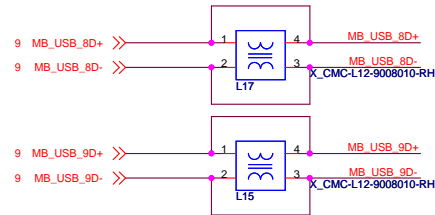
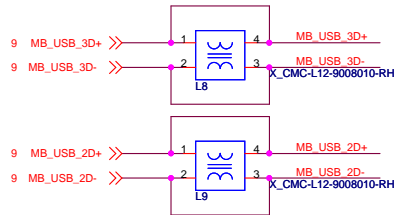
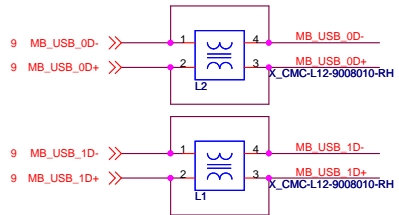


**FRONT USB PORT2,3**

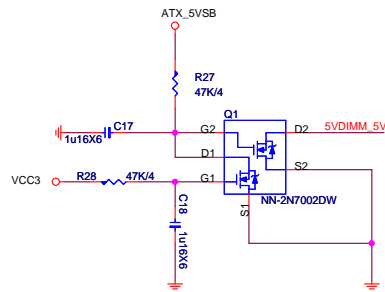
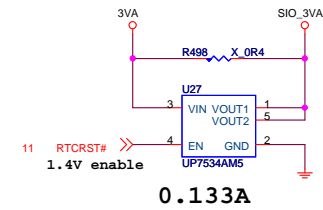
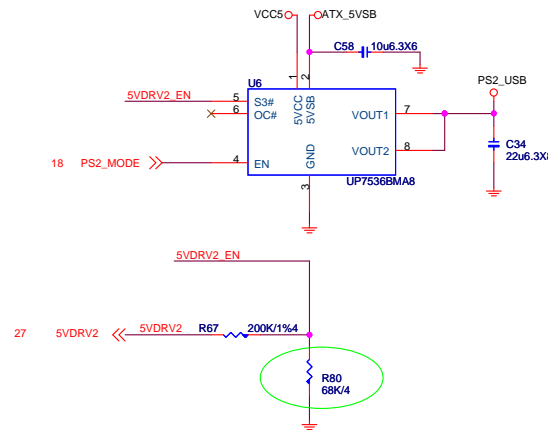
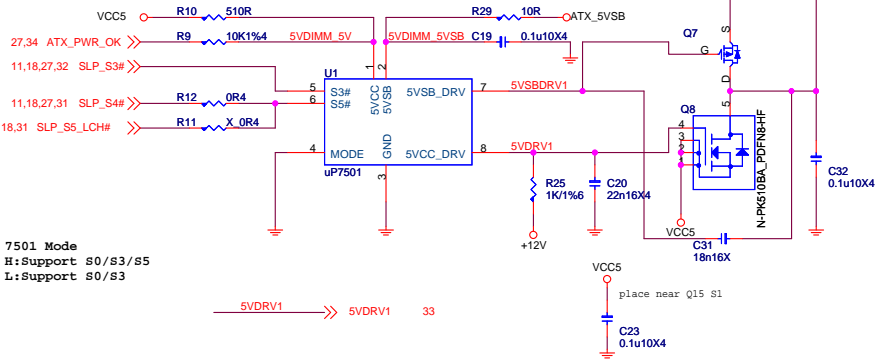
**FRONT USB PORT4,5(With Lan)**

**FRONT USB PORT8,9**

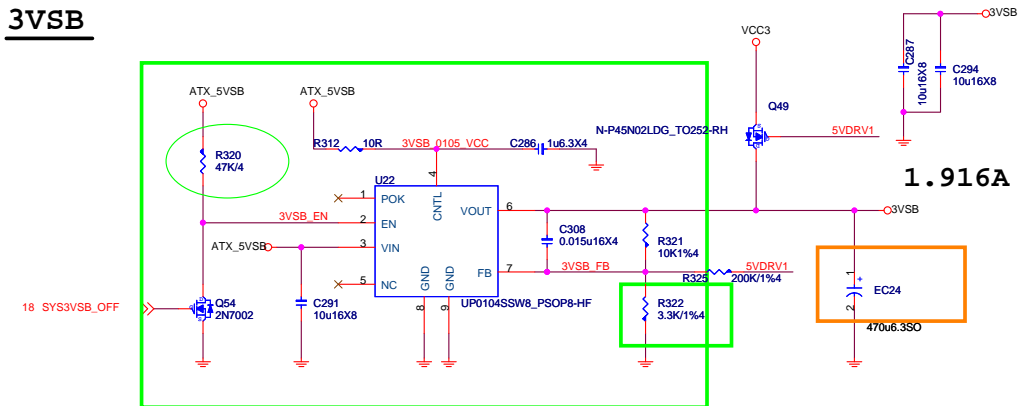
**FRONT USB PORT 10,11**



## 5VDIMM FOR DDR

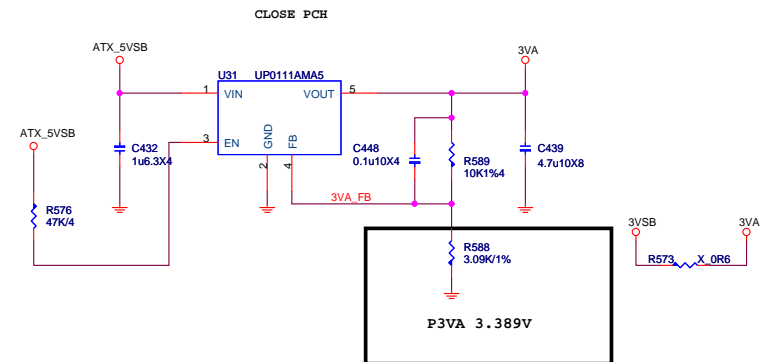


## 3VSB



## 3VA

20mA

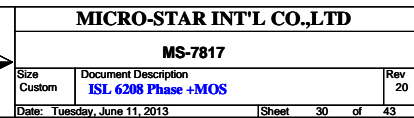


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# DDR Power:1.5V

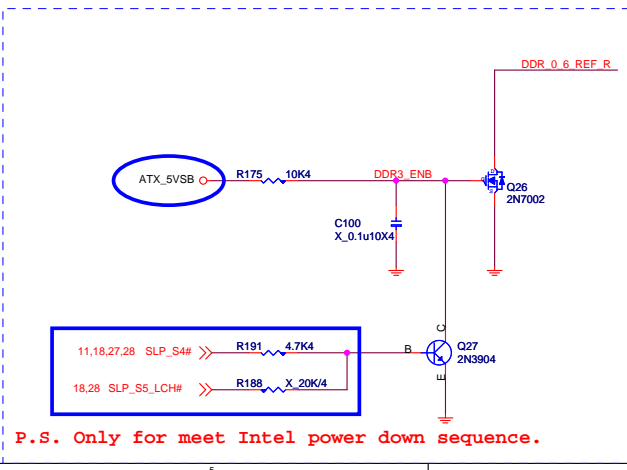
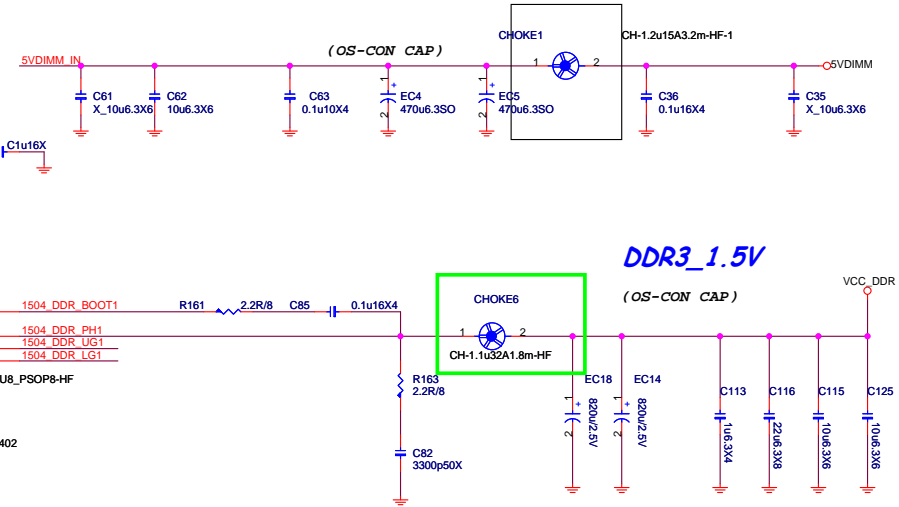
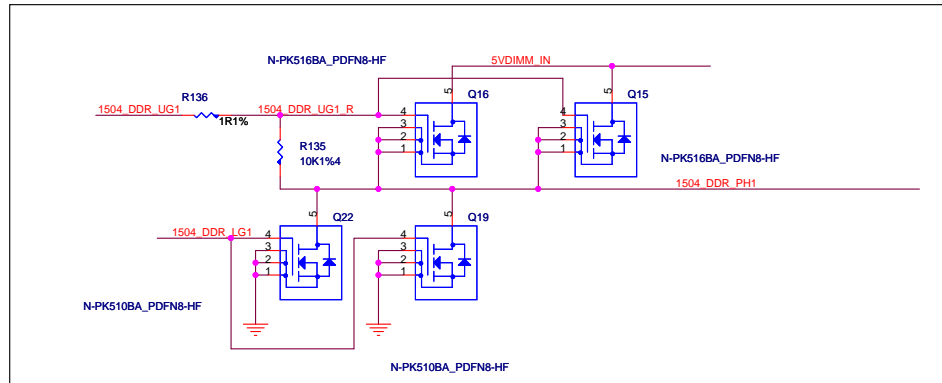
DDR3\_1.5V ICCMAX 23.6A

4.5A FOR CPU  
12A FOR 4DIMM  
1.1A FOR DDR VTT  
6A FOR PCH\_1P05

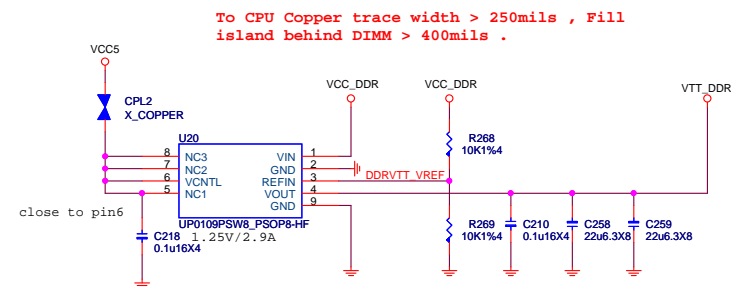
Tripple=9.6  
 $4.7*2*1=9.4A<9.6A$

OCp  $23.6*1.5=35A$   
 $35A=(20uA*Rocs(R142))/4*Rdson(Low\ side1.65mohm)$   
 $R142=11.9K\ ohm$

$$((R221/R226)+1)*0.6=1.5V$$

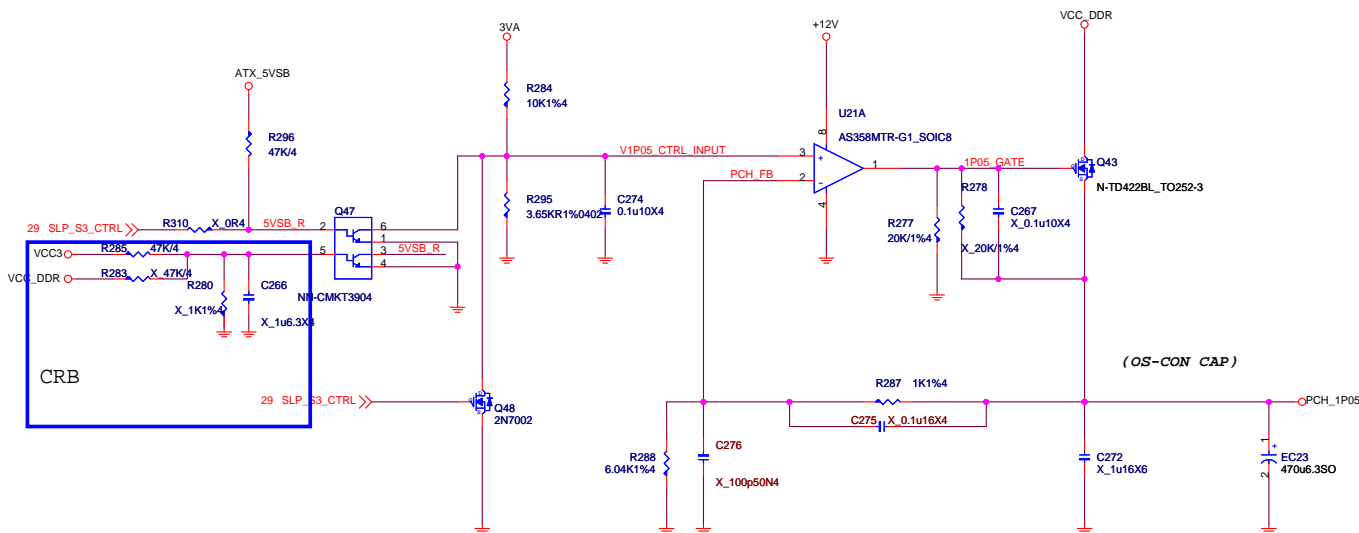


## DDR VTT Power

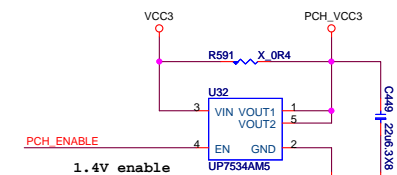


To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

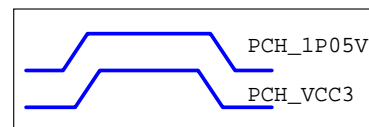
**PCH Power:1.05V 5.747A**



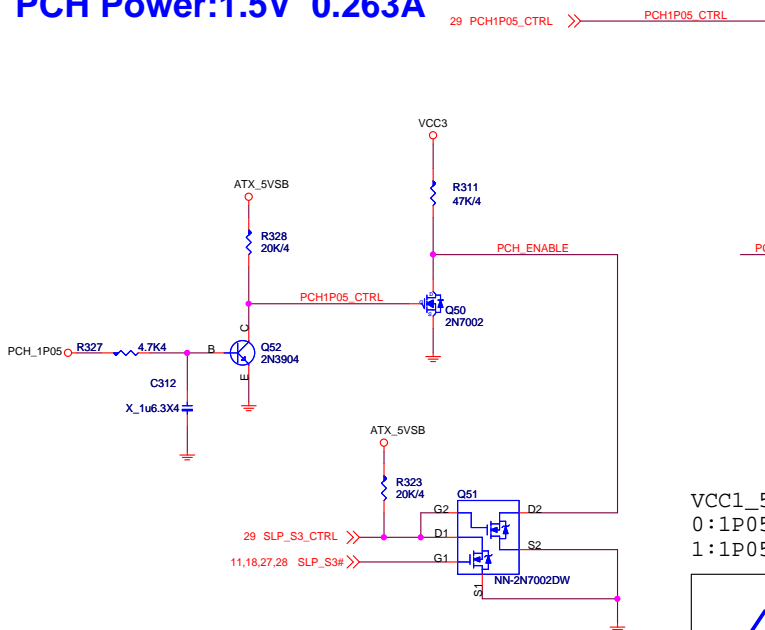
0.133A



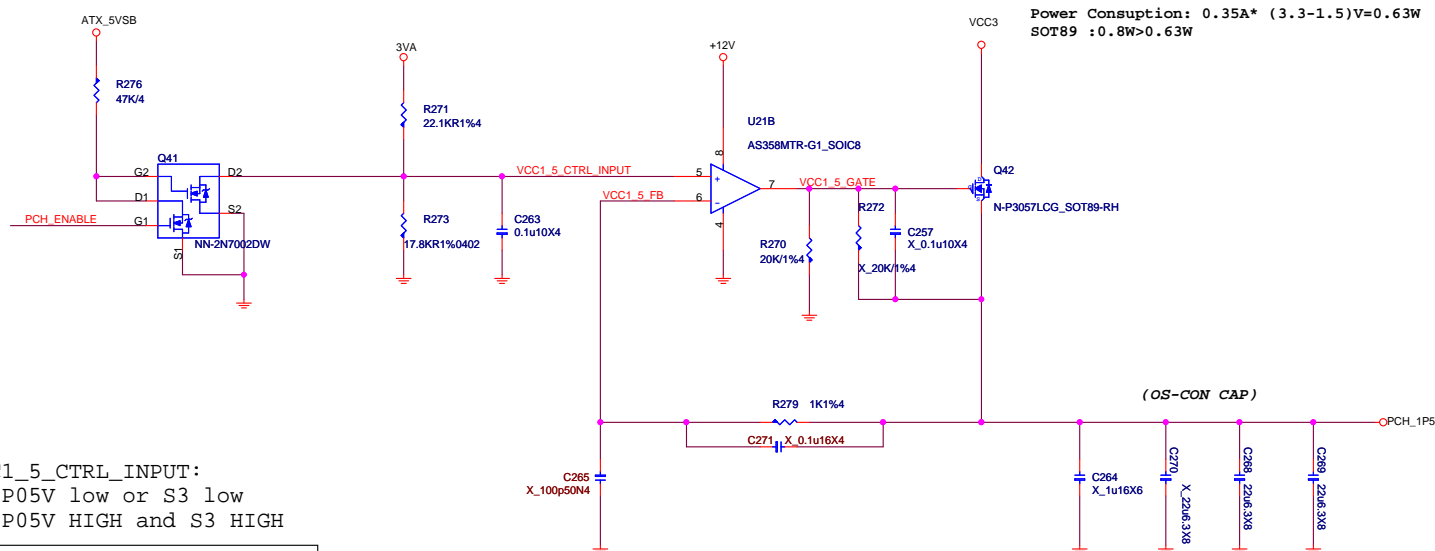
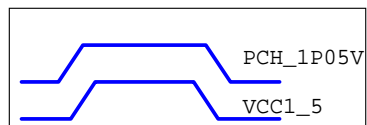
```
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH
```



**PCH Power:1.5V 0.263A**



```
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH
```



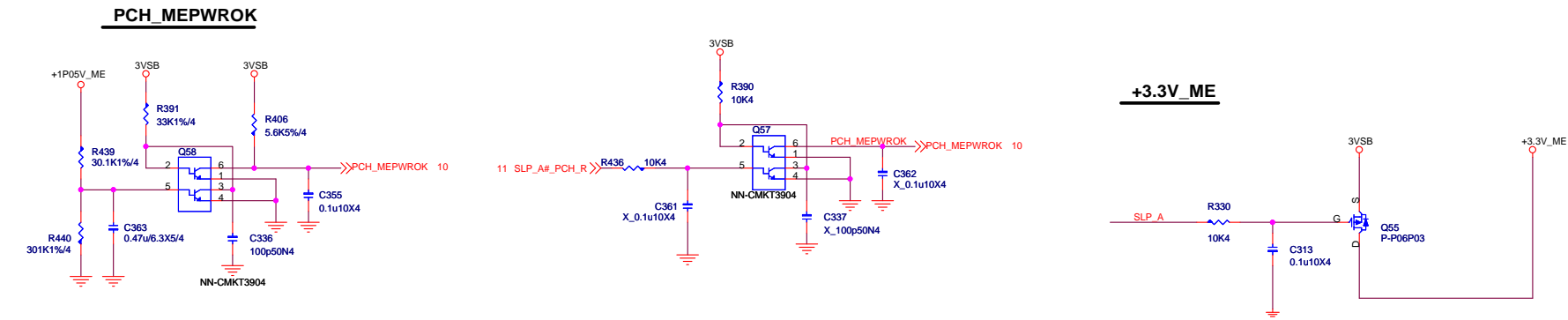
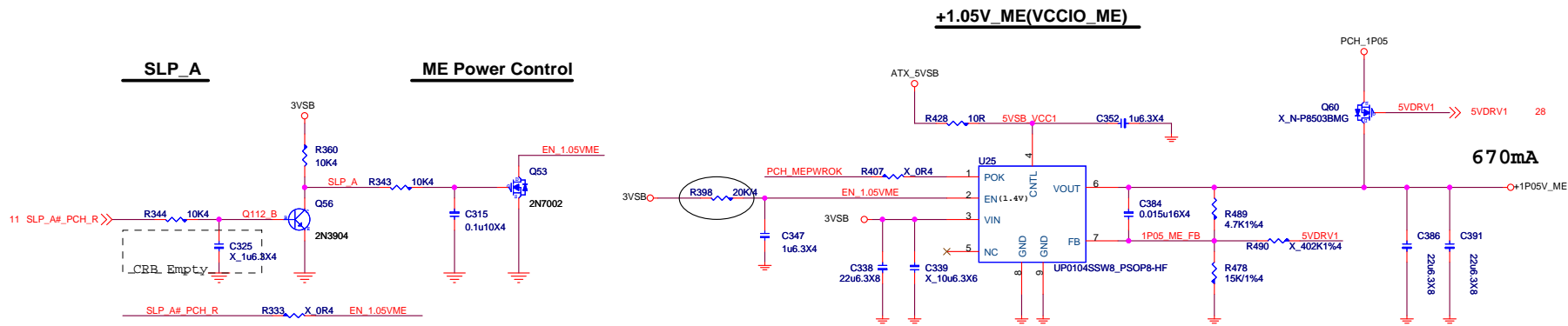
Power Consuption:  $0.35A * (3.3-1.5)V = 0.63W$   
SOT89 :  $0.8W > 0.63W$

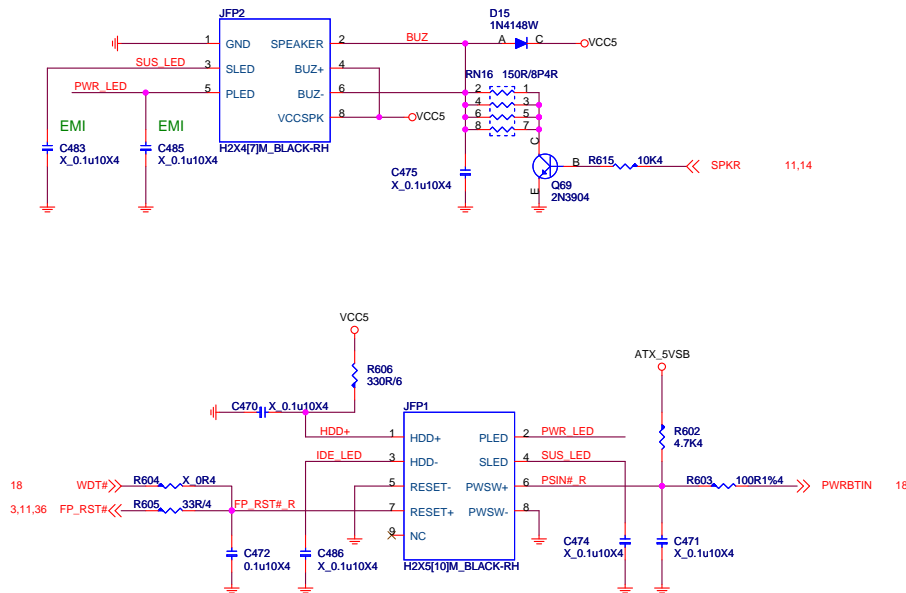


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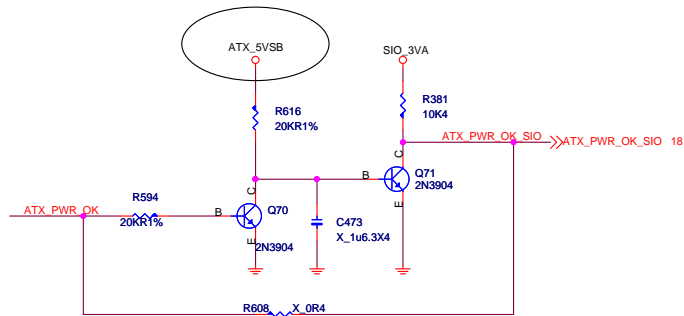
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[illegible]

Reserve pull high to 5VDIMM if PM don't want PLED light in deep mode.



D14 1N4148W  
 VCC5 A C LPT VC

C476 0.1u10X4

R15 33R/8P4R R22 2.7K/8P4R  
 PPRND0 1 2 PRND0 8 7  
 PPRND13 4 PRND1 6 5  
 PPRND25 6 PRND3 4 3  
 PPRND37 8 PRND3 2 1

R19 33R/8P4R R20 2.7K/8P4R  
 PPRND4 7 8 PRND4 8 7  
 PPRND5 5 6 PRND5 6 5  
 PPRND6 3 4 PRND6 4 3  
 PPRND7 1 2 PRND7 2 1

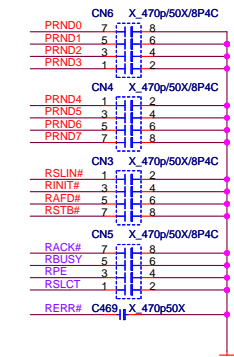
R17 33R/8P4R R18 2.7K/8P4R  
 STB# 1 2 RSTB# 8 7  
 AFD# 3 4 RAFD# 6 5  
 INIT# 5 6 RINIT# 4 3  
 SLIN# 7 8 RSLIN# 2 1

R21 2.7K/8P4R  
 RACK# 8 7  
 RBUSY 6 5  
 RPE 4 3  
 RSLCT 2 1

RERR# R601 2.7K/1%4

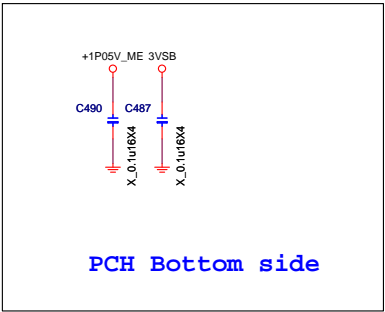
JLP1  
 RSTB# 1 2 RAFD#  
 PRND0 3 4 RERR#  
 PRND1 5 6 RINIT#  
 PRND2 7 8 RSLIN#  
 PRND3 9 10  
 PRND4 11 12  
 PRND5 13 14  
 PRND6 15 16  
 PRND7 17 18  
 RACK# 19 20  
 RBUSY 21 22  
 RPE 23 24  
 RSLCT 25

HZXT3261M\_BLACK-RH

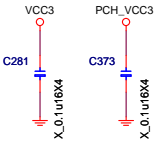


TPM pinout diagram for HX2710J0M-2PITCH. The diagram shows a 14-pin connector with pins 1-14. Pin 1 is TPM\_CLK, Pin 2 is PLTRST\_BU1#, Pin 3 is LPC\_AD0, Pin 4 is LPC\_AD1, Pin 5 is LPC\_AD2, Pin 6 is LPC\_AD3, Pin 7 is LPC\_FRAME#, Pin 8 is JTPM1, Pin 9 is VCC3, Pin 10 is VCC5, Pin 11 is SERIRQ\_R, Pin 12 is VCC5, Pin 13 is VCC5, and Pin 14 is GND. The diagram also shows a 3VSB supply connected to pin 1, a VCC3 supply connected to pin 2, a VCC5 supply connected to pin 10, and a GND connection to pin 14. The diagram is labeled 'add 0607'.



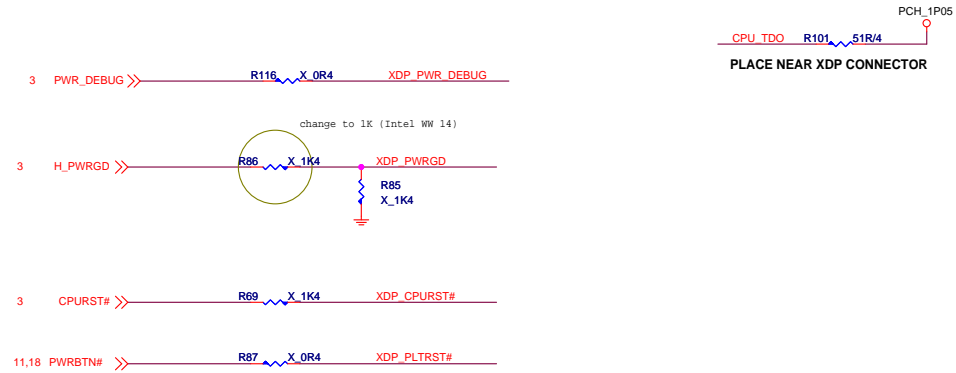
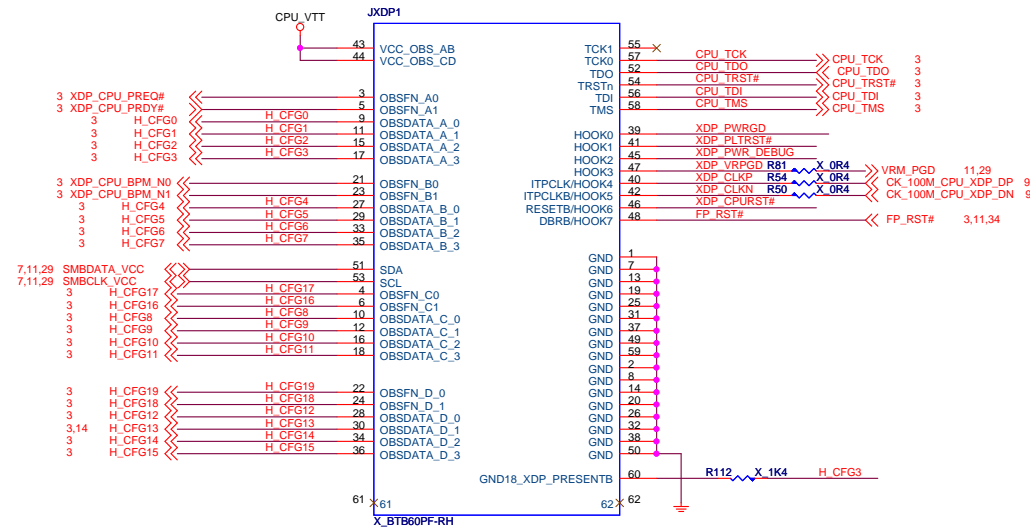


PCH Bottom side



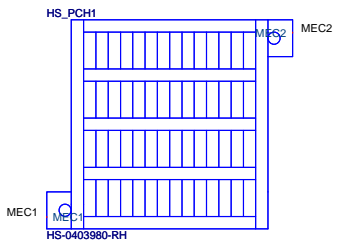
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# Reserve debug port 5020

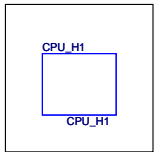
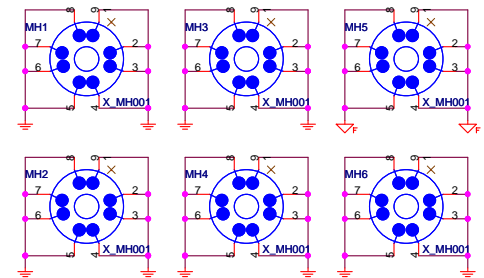


5 4 3 2 1

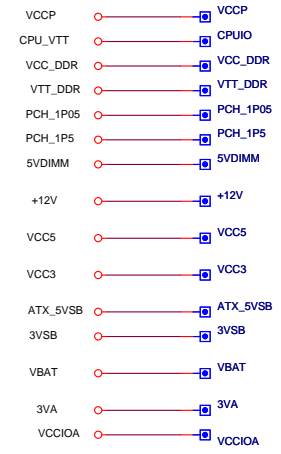
Voltage test point



Mounting Holes



PK0-0781721-G37, 精成, 23, 寶安恩斯邁廠 (MSIS)  
PK0-0781721-R48, 競華, 23, 寶安恩斯邁廠 (MSIS)



Optical Fiducial Marks-120

Simulation

